

Fig. 1

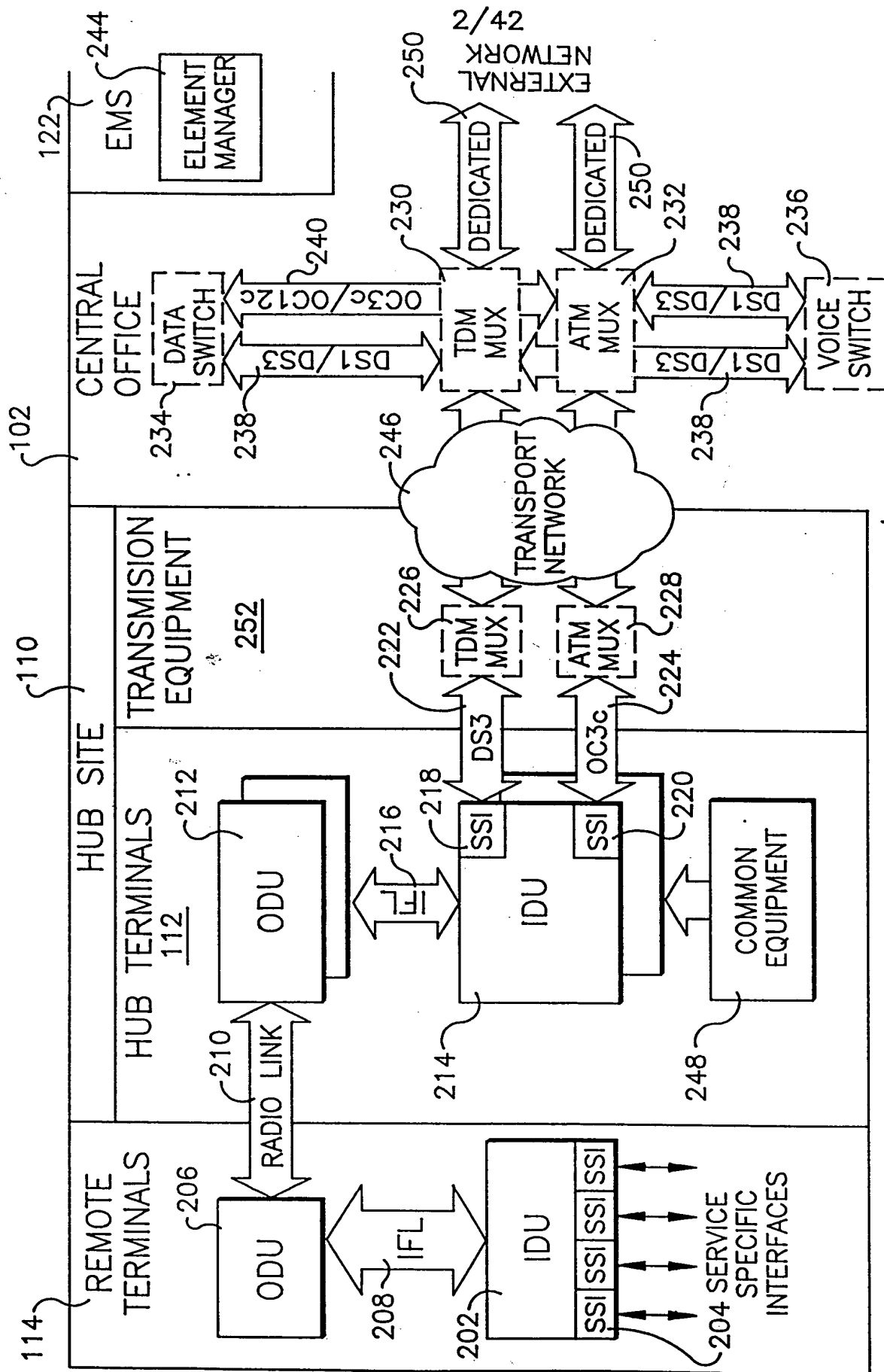


Fig. 2

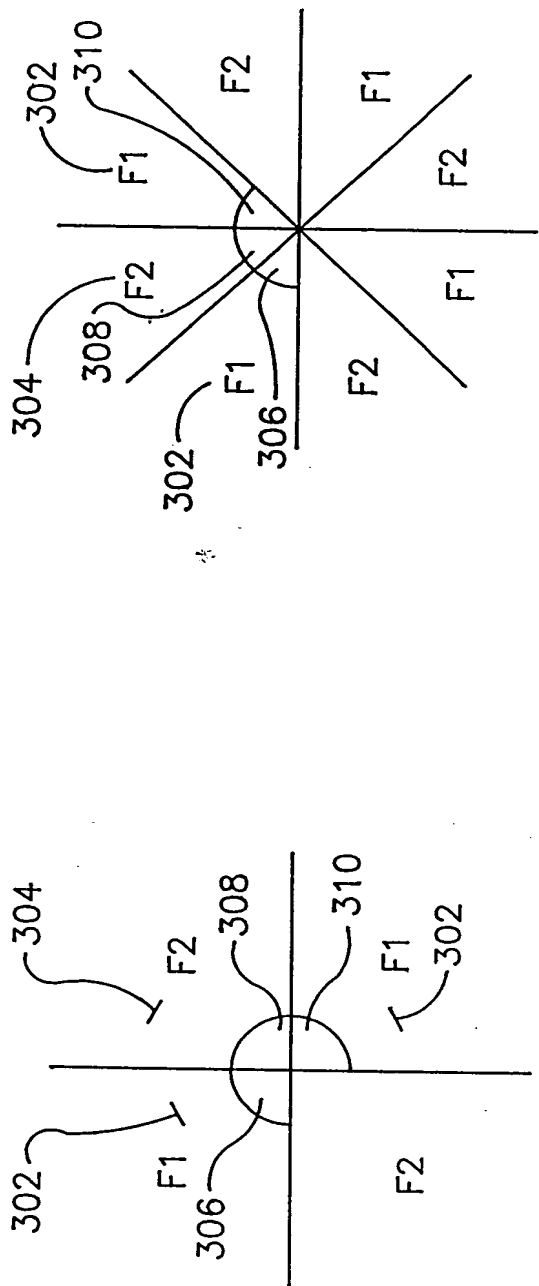


Fig. 3A

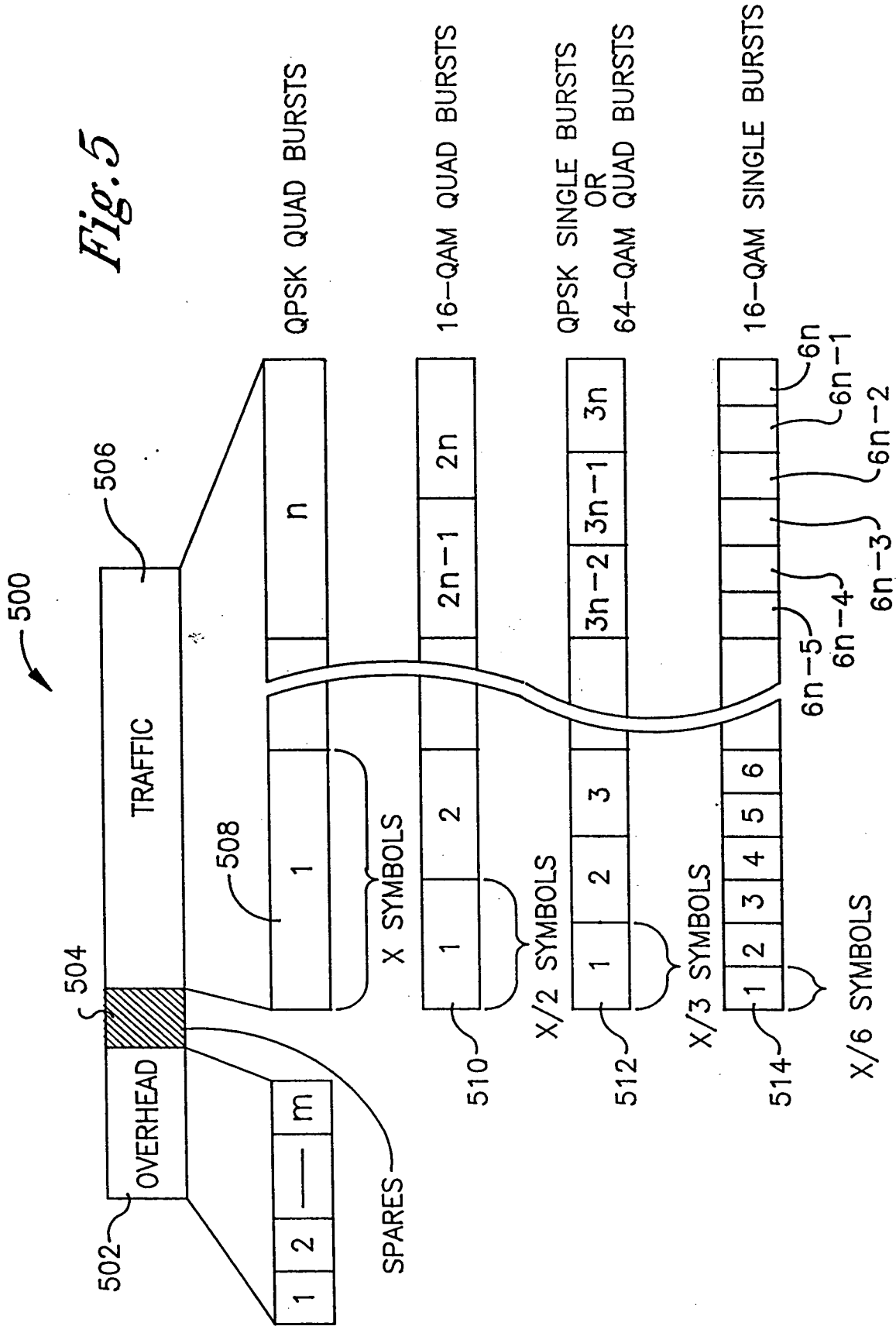
Fig. 3B

400

402

FRAME 1	FRAME 2	FRAME 3		FRAME N-1	FRAME N
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Fig. 4



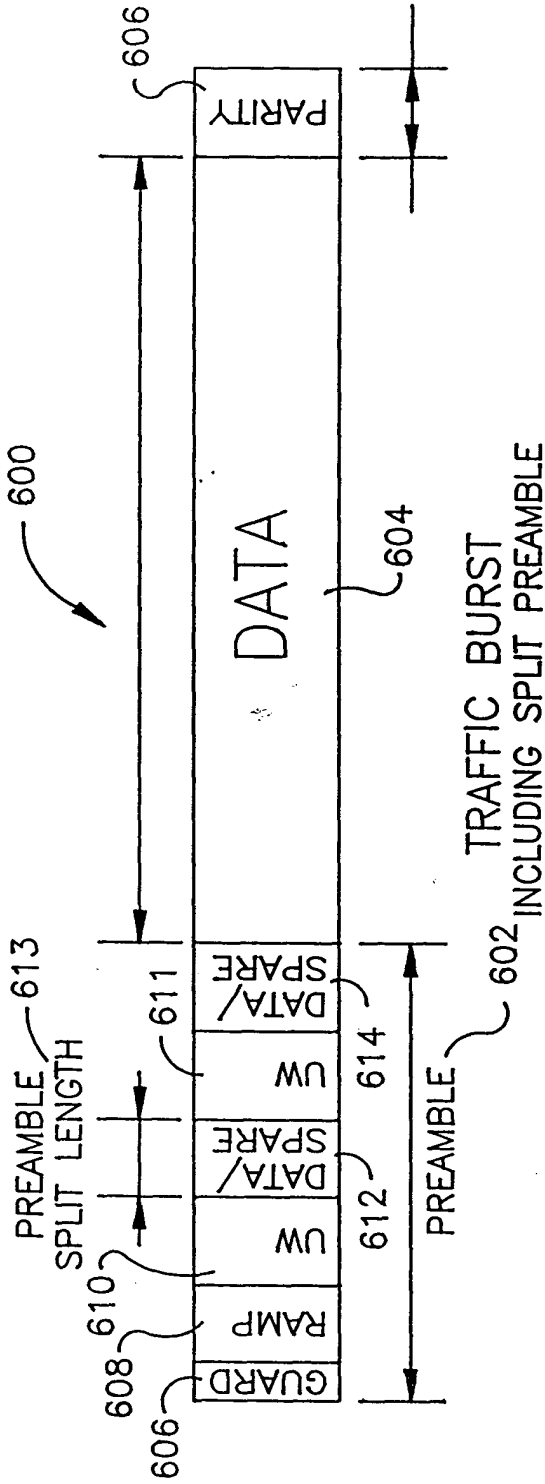


Fig. 6

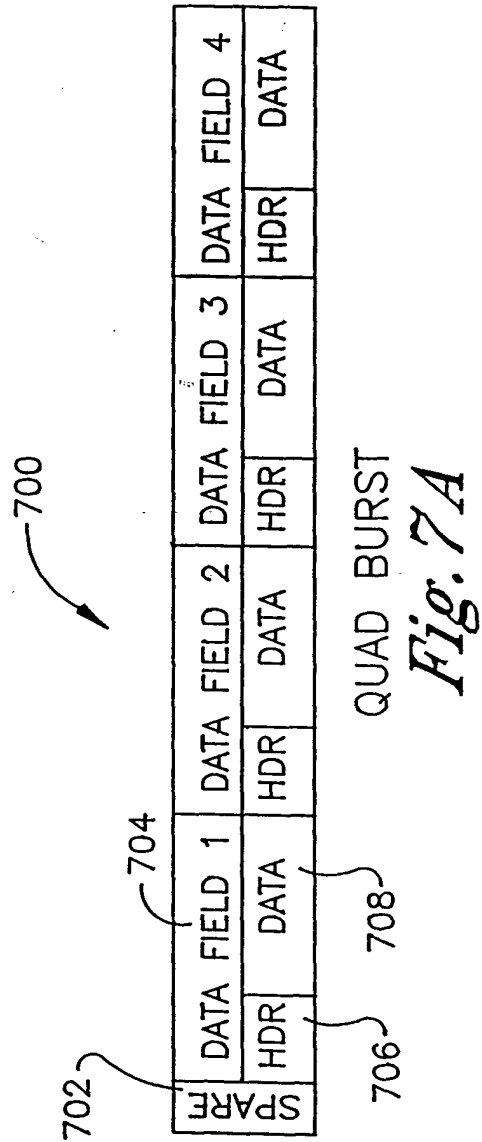


Fig. 7A

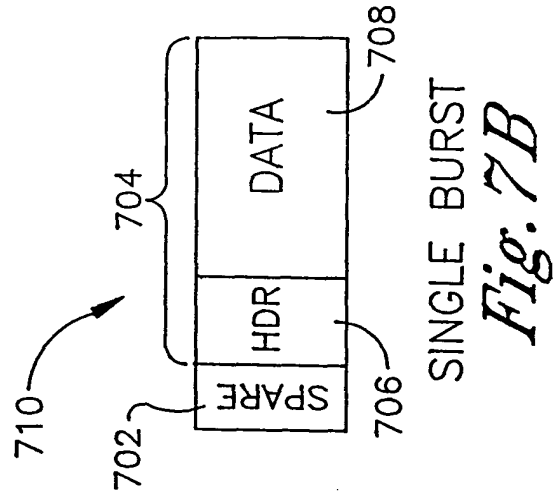


Fig. 7B

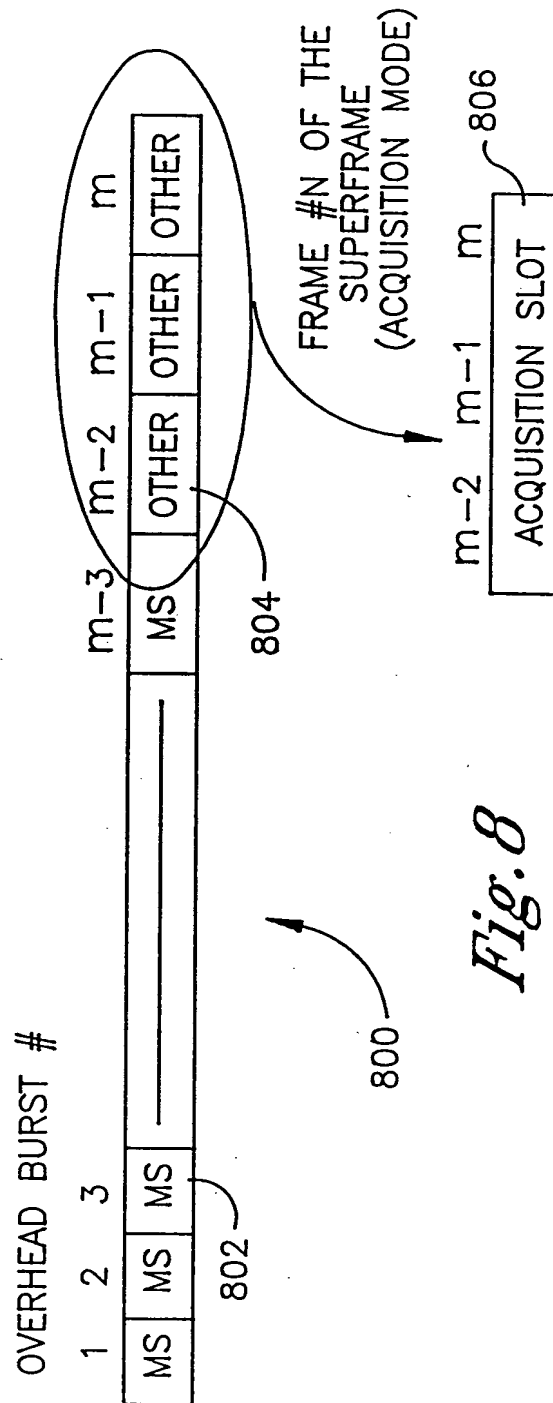


Fig. 8

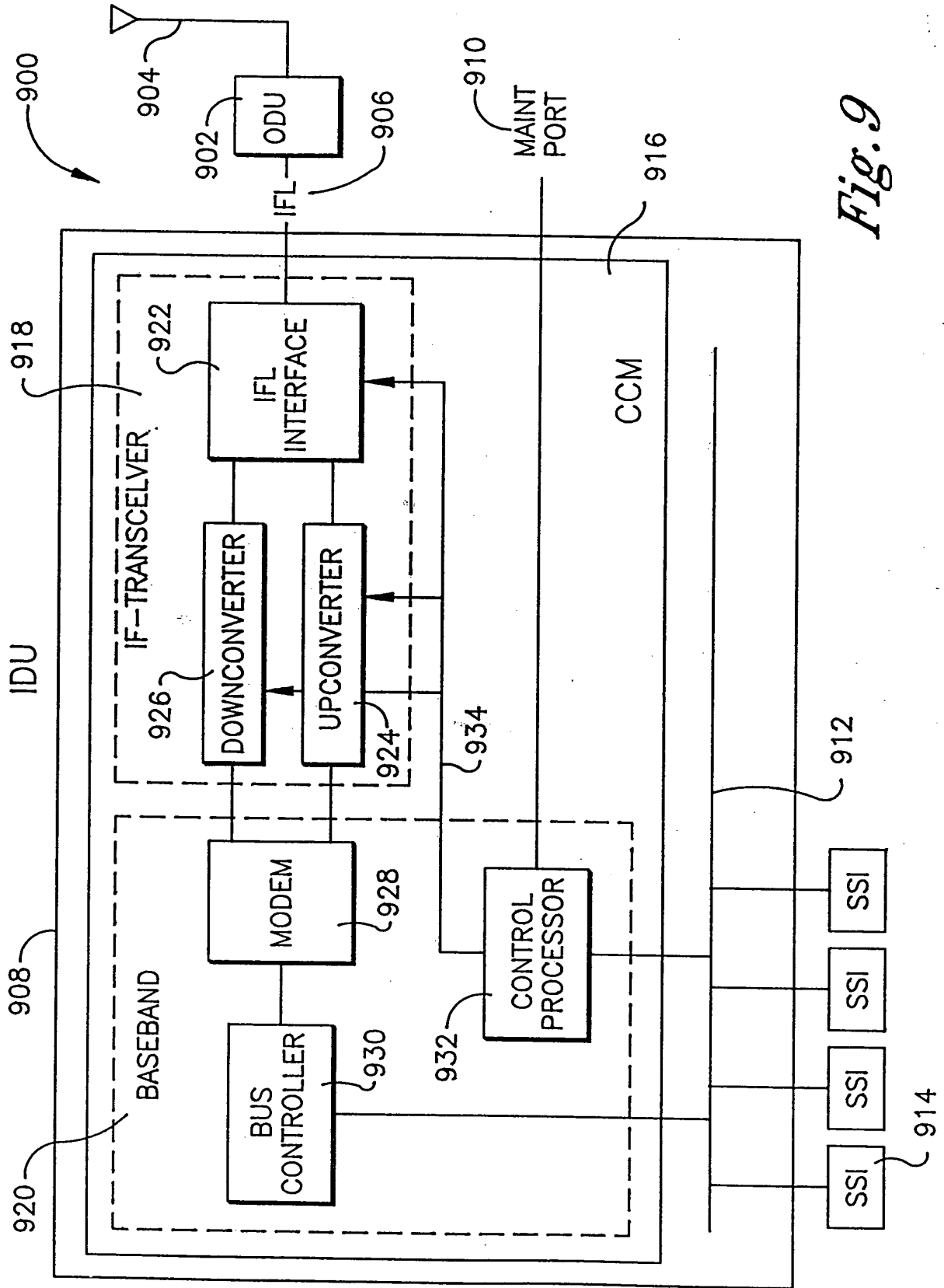


Fig. 9

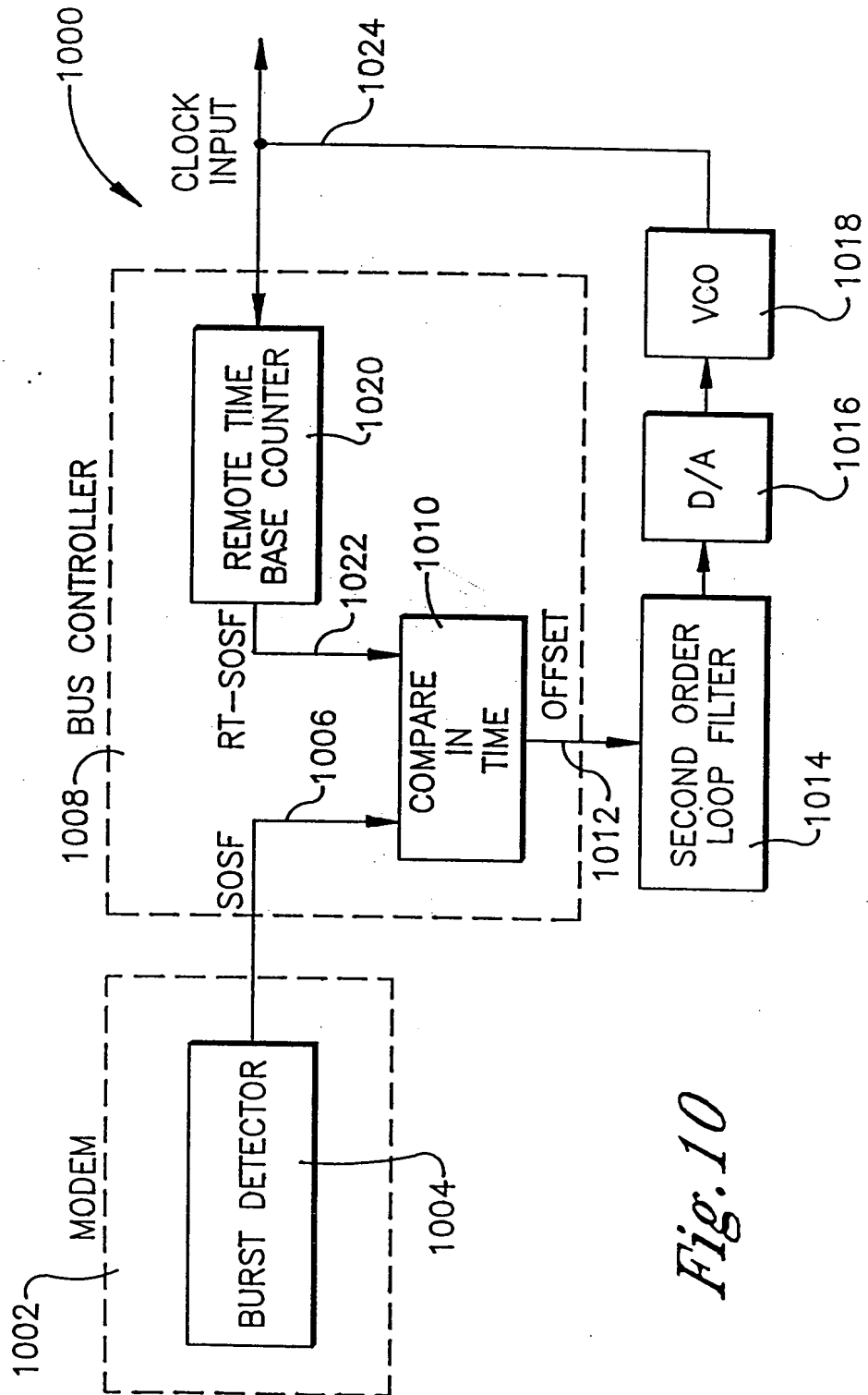


Fig. 10

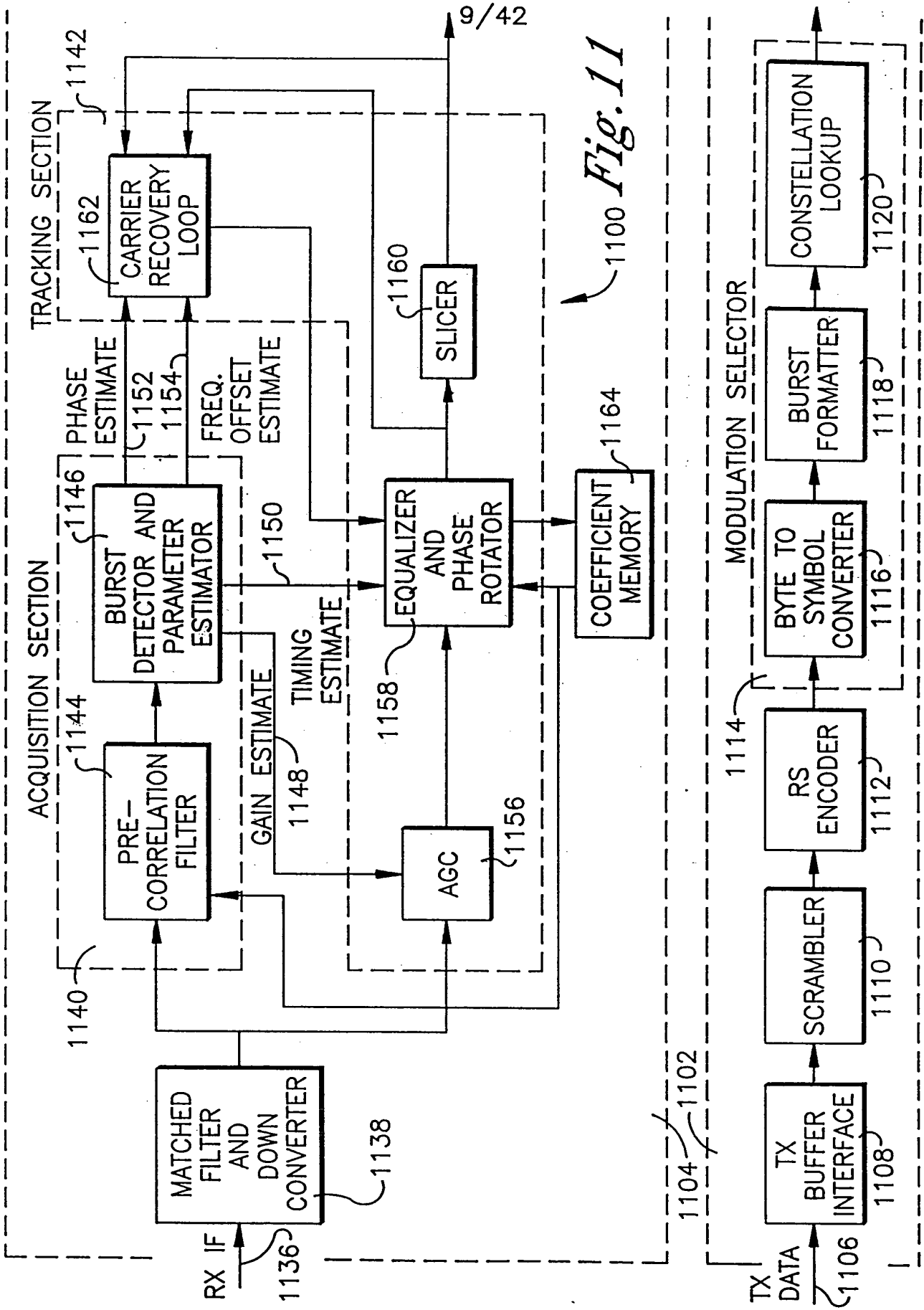
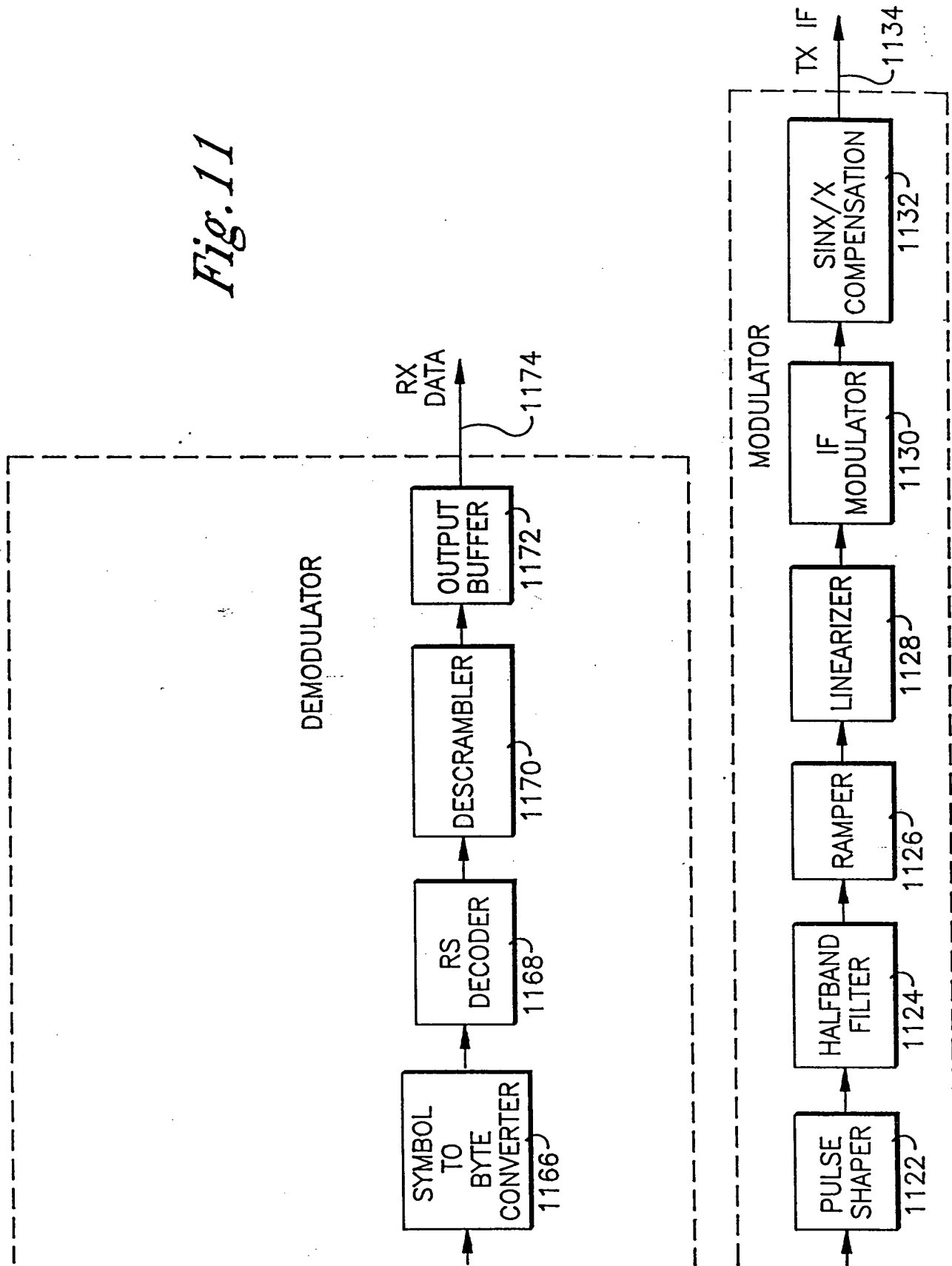
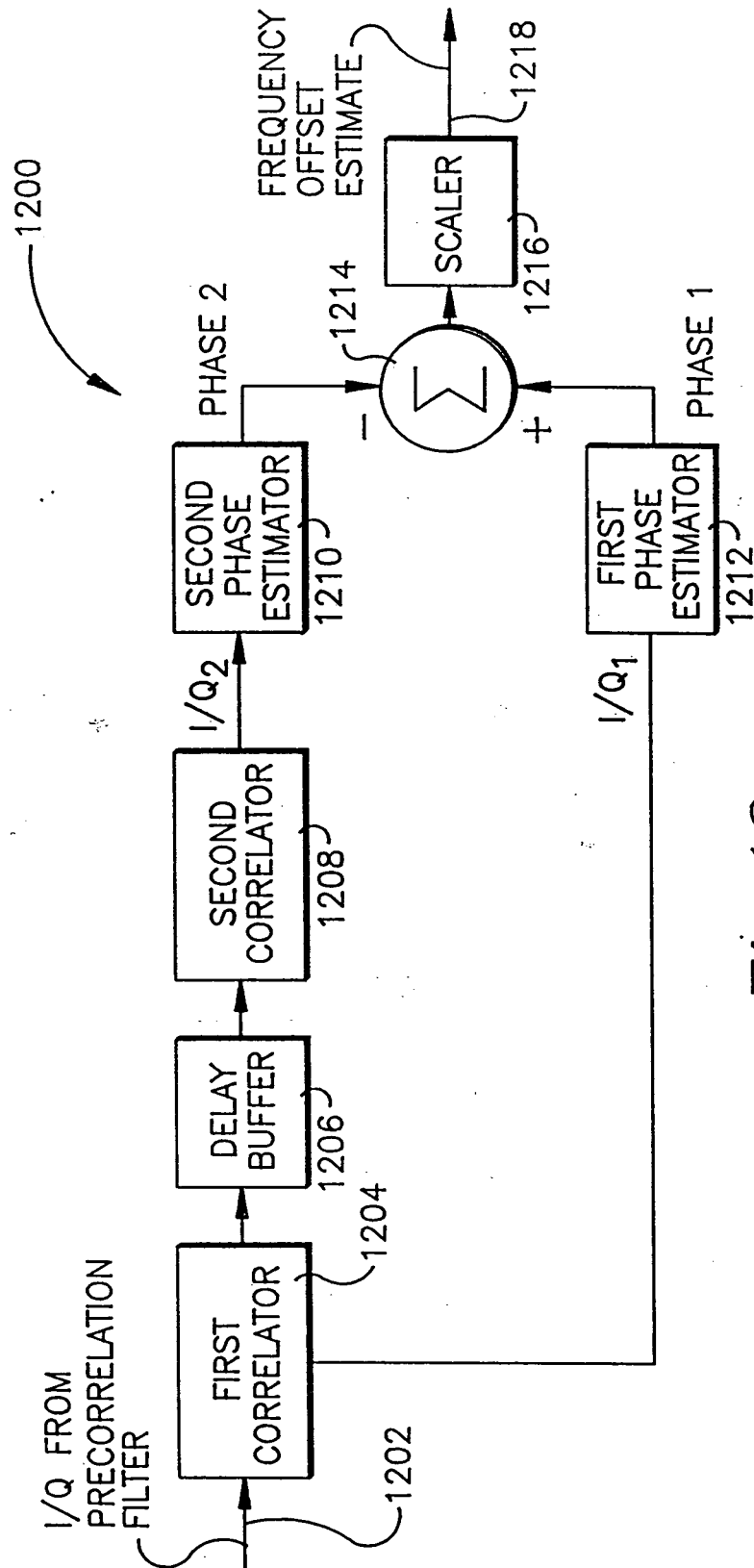
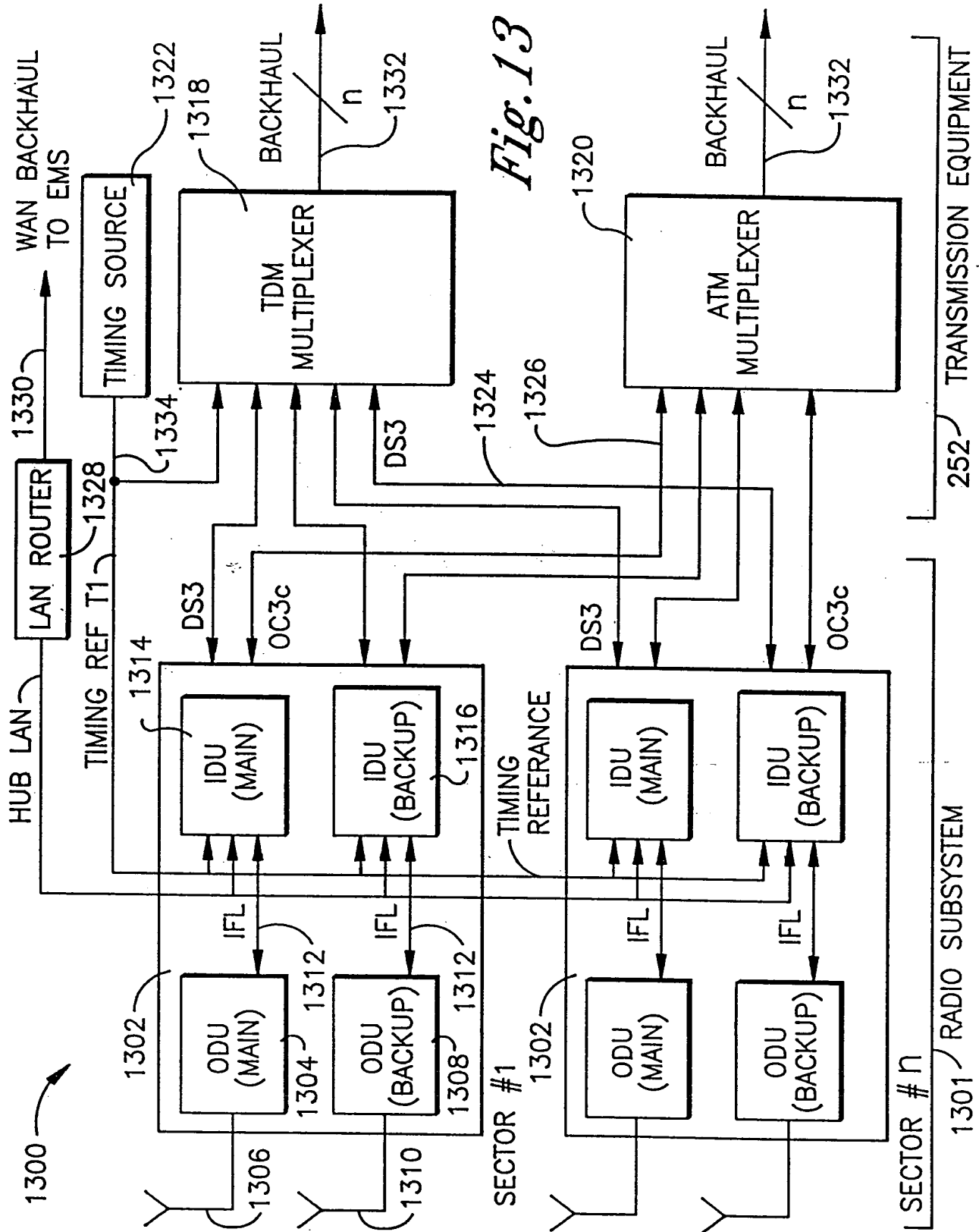


Fig. 11

Fig. 11





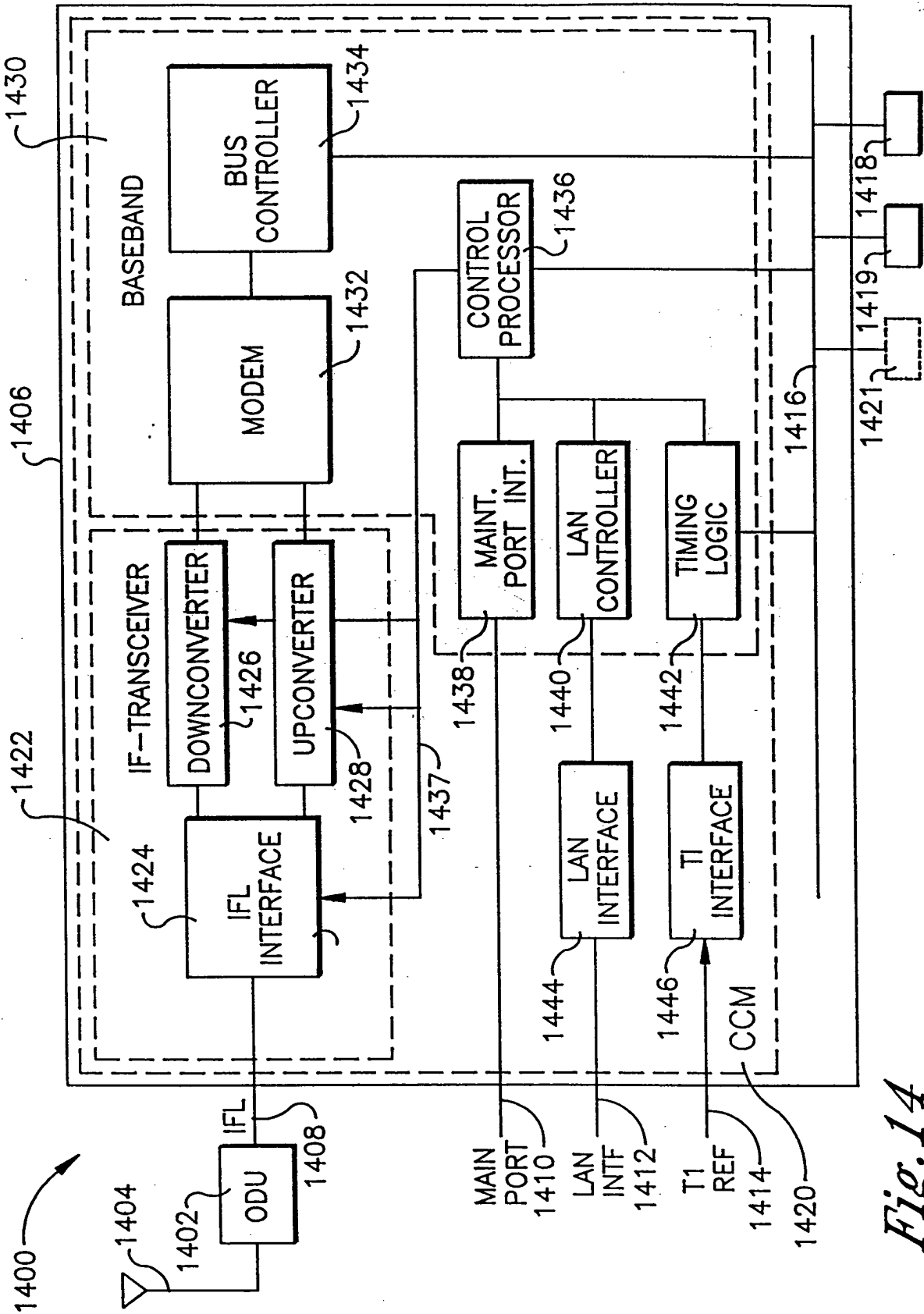
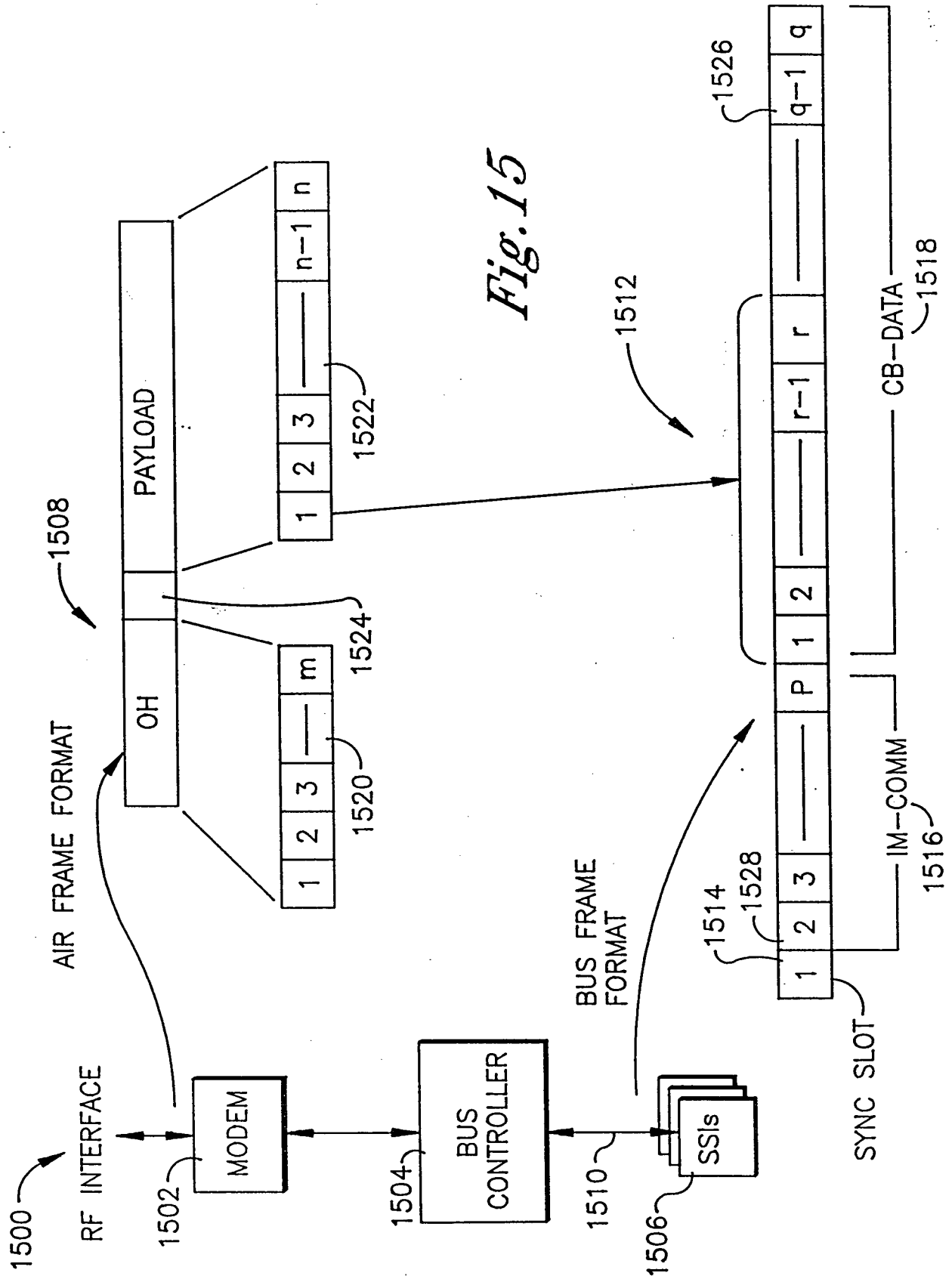


Fig. 14



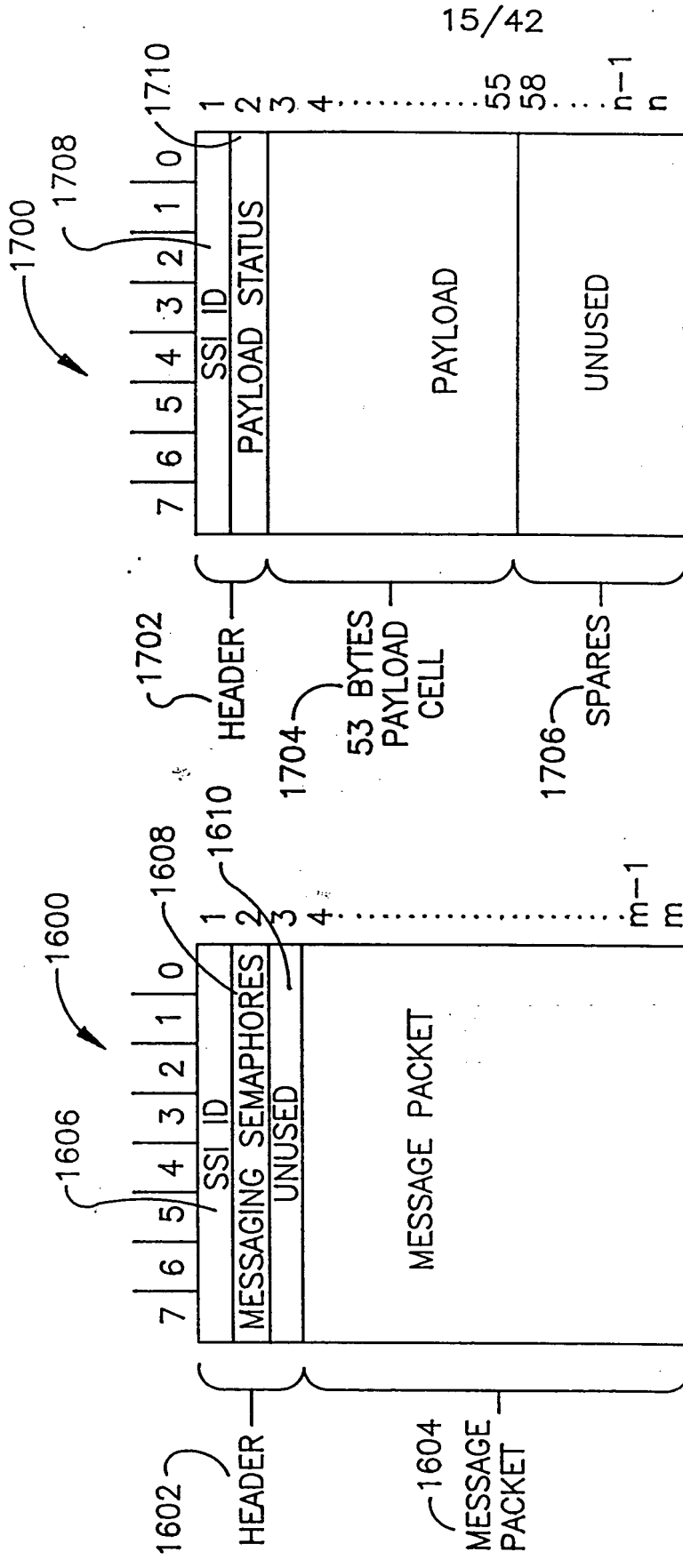


Fig. 16

Fig. 17

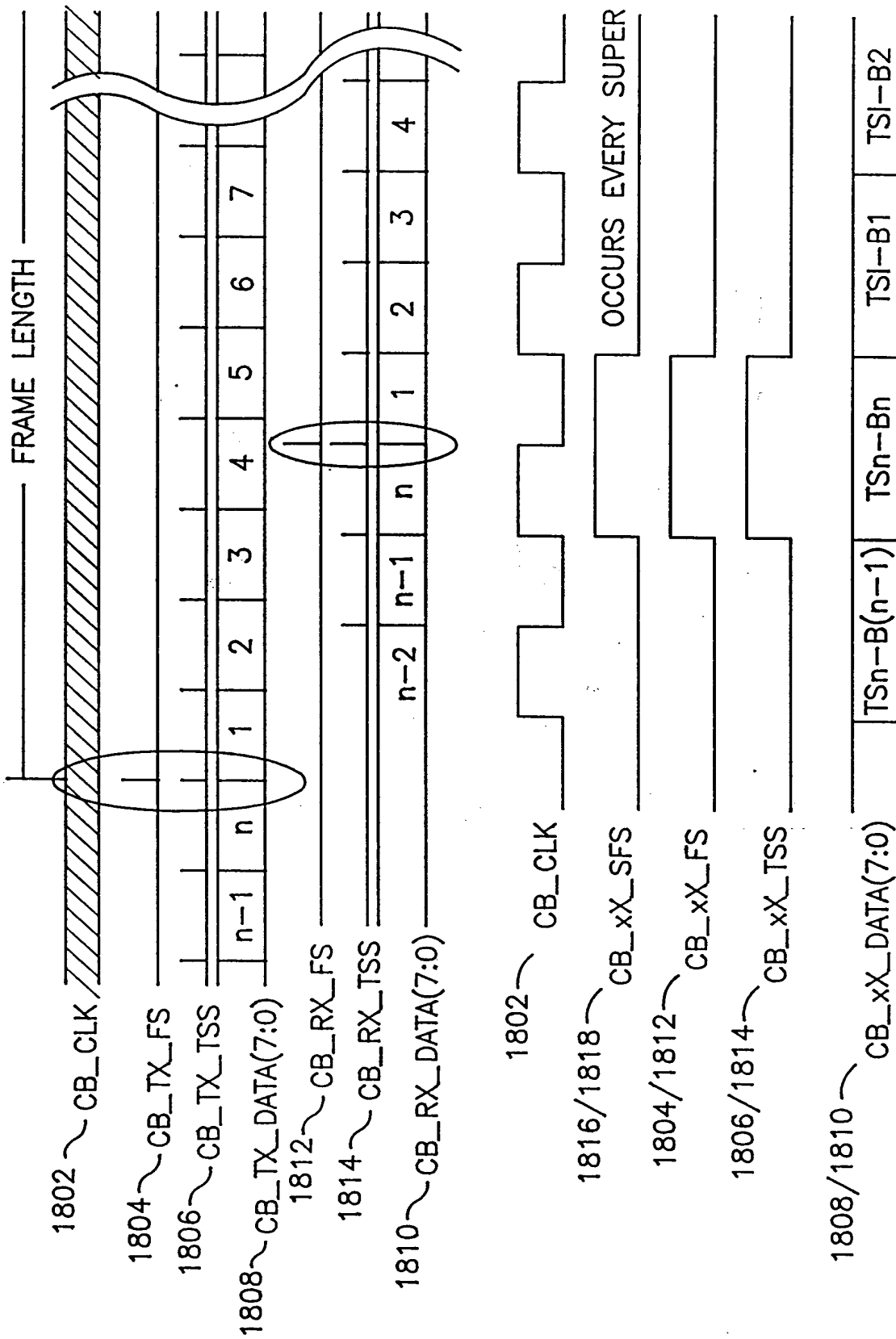


Fig. 18 CELL BUS TIMING

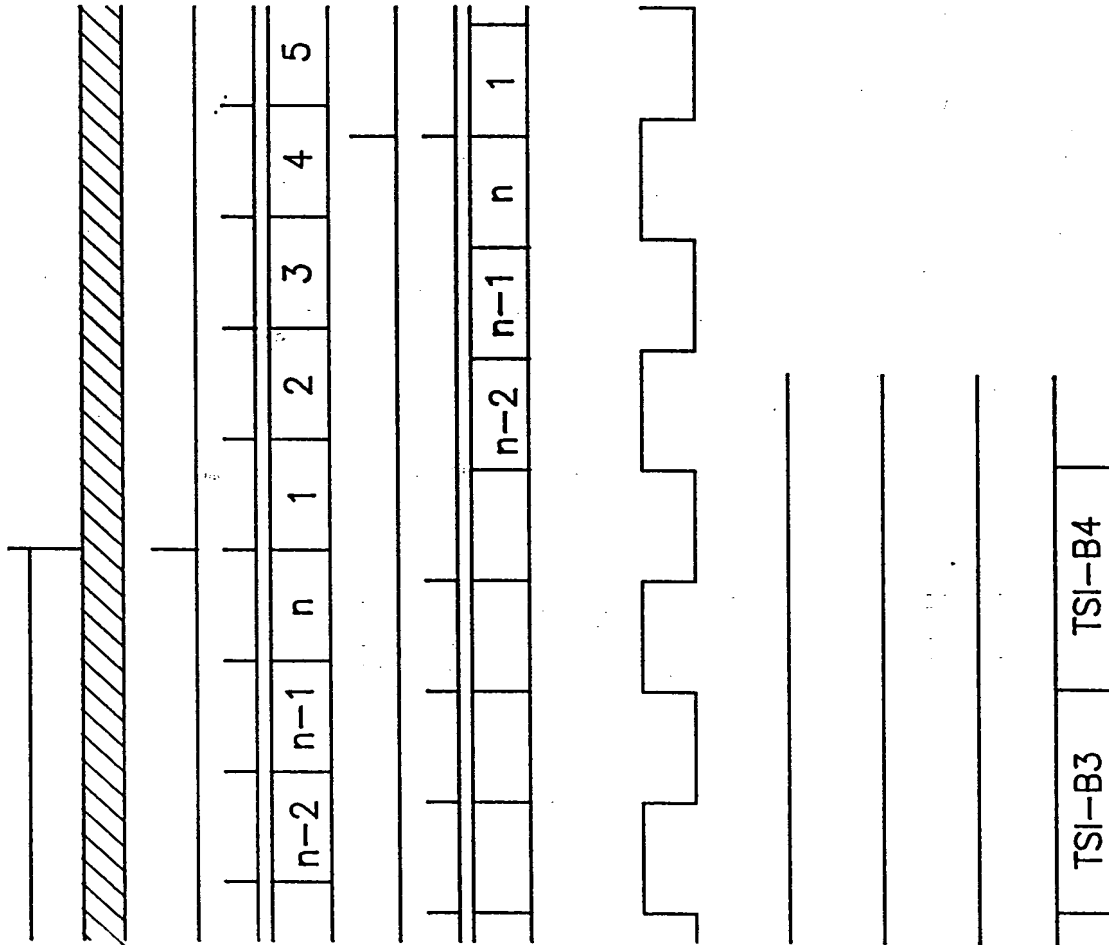
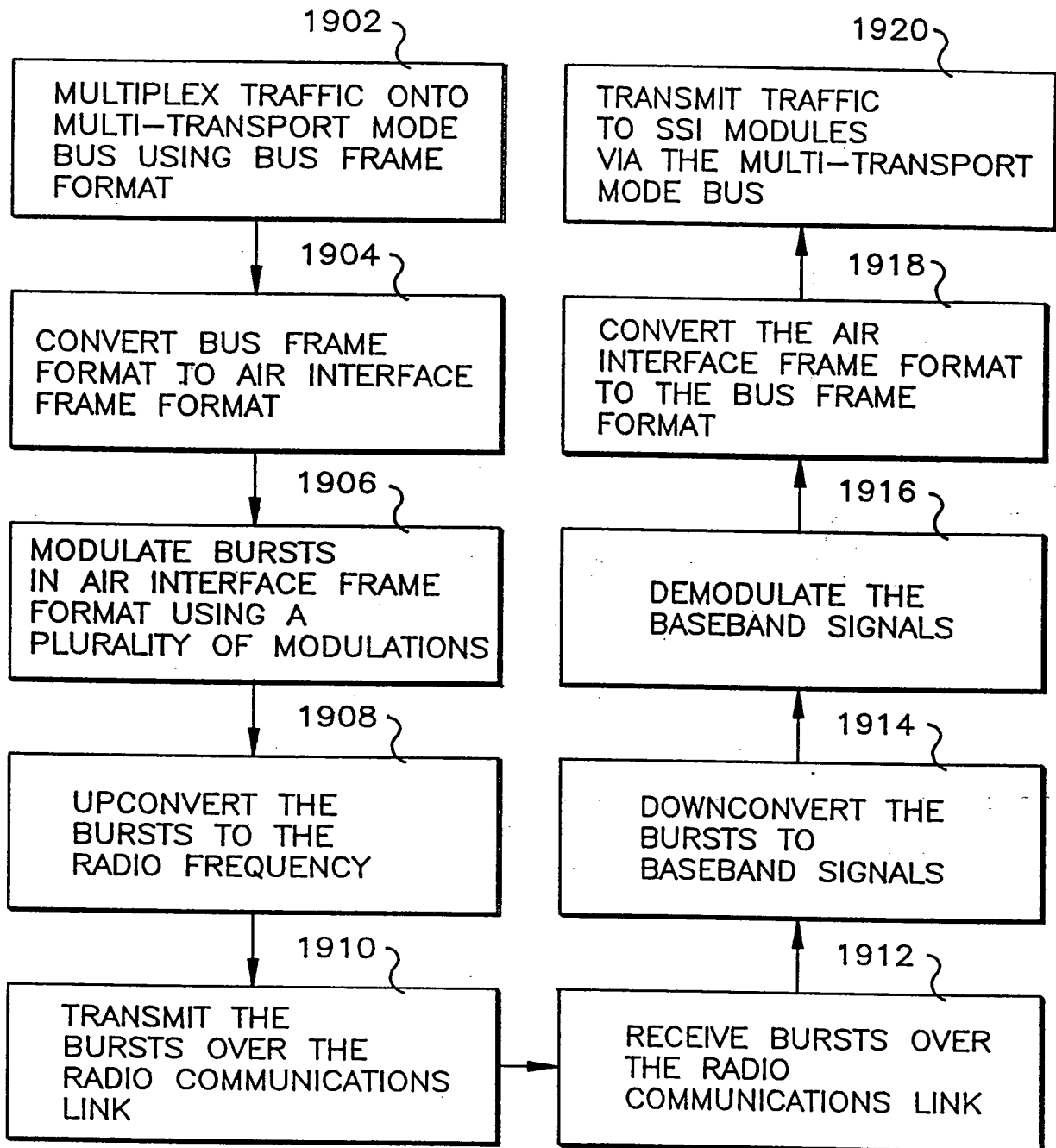


Fig. 18

*Fig. 19*

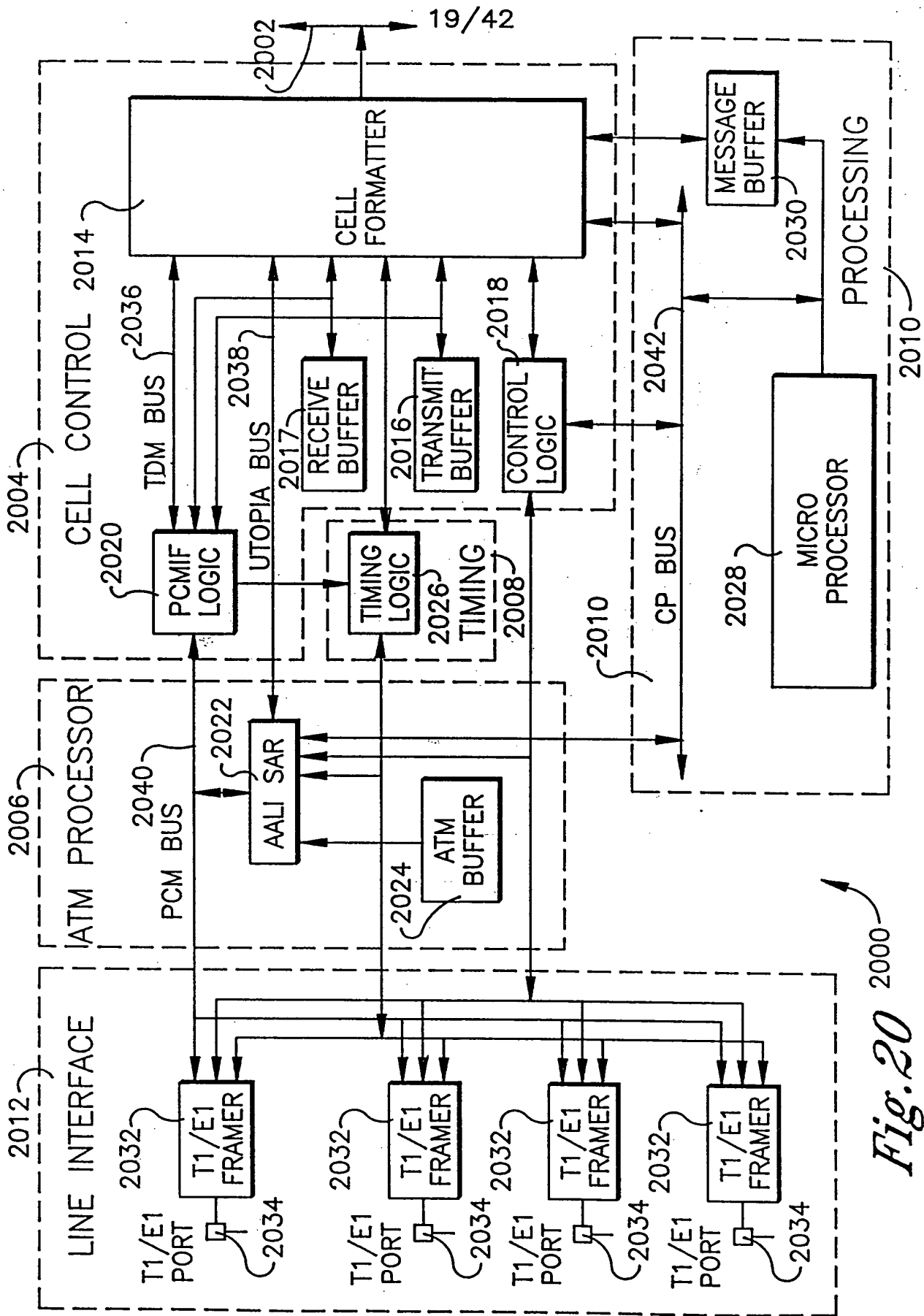


Fig. 20

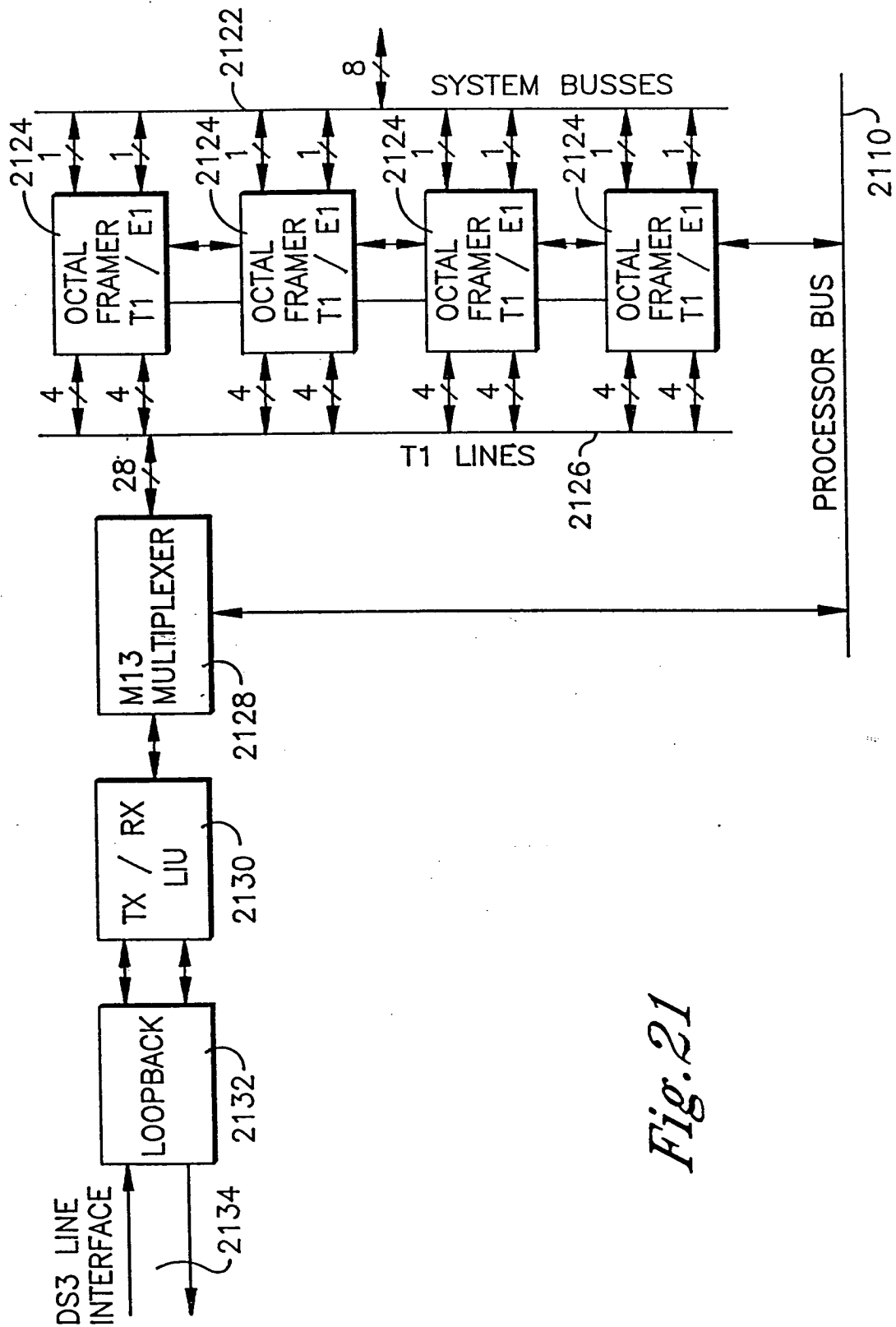
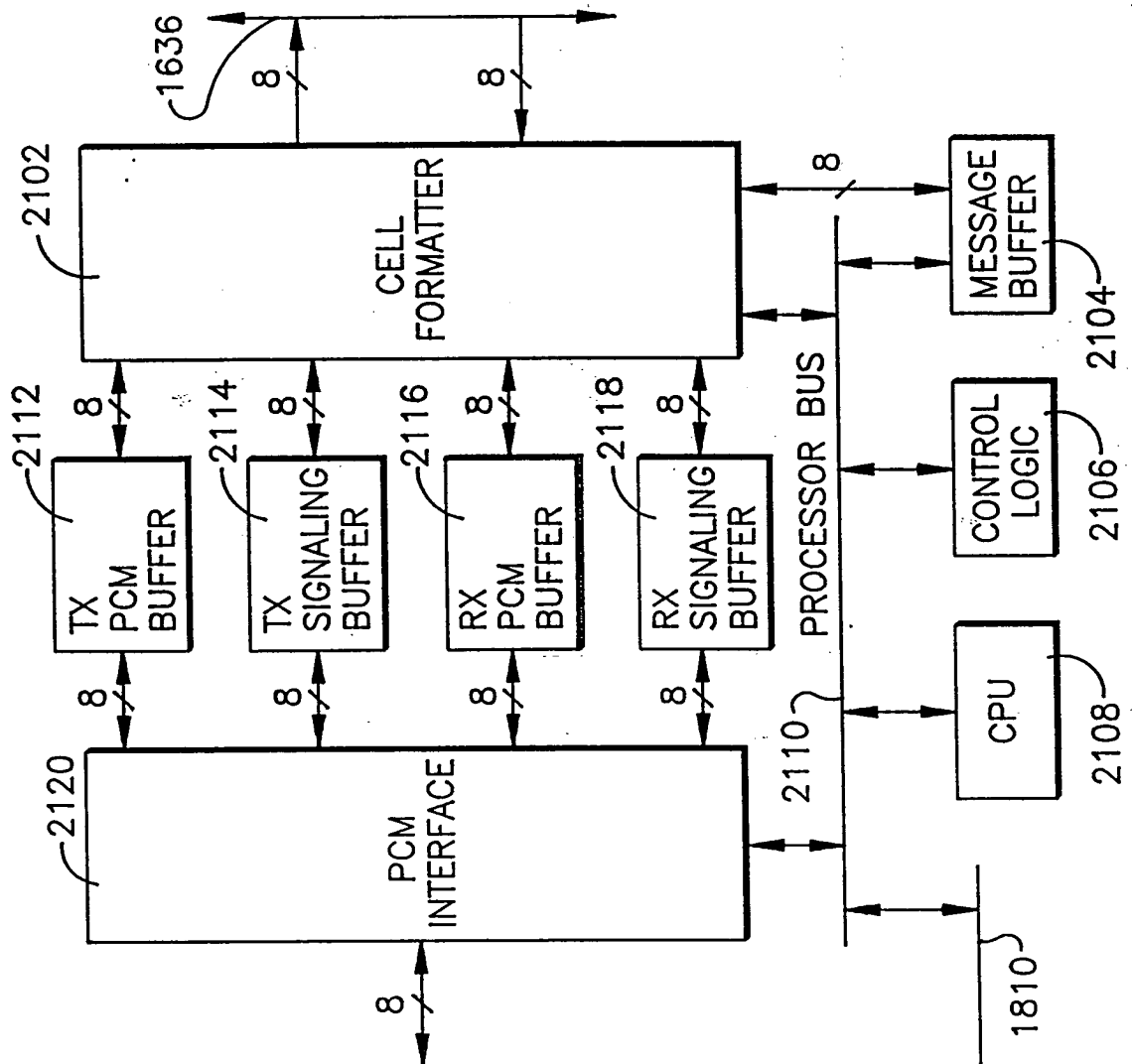


Fig. 21

Fig. 21



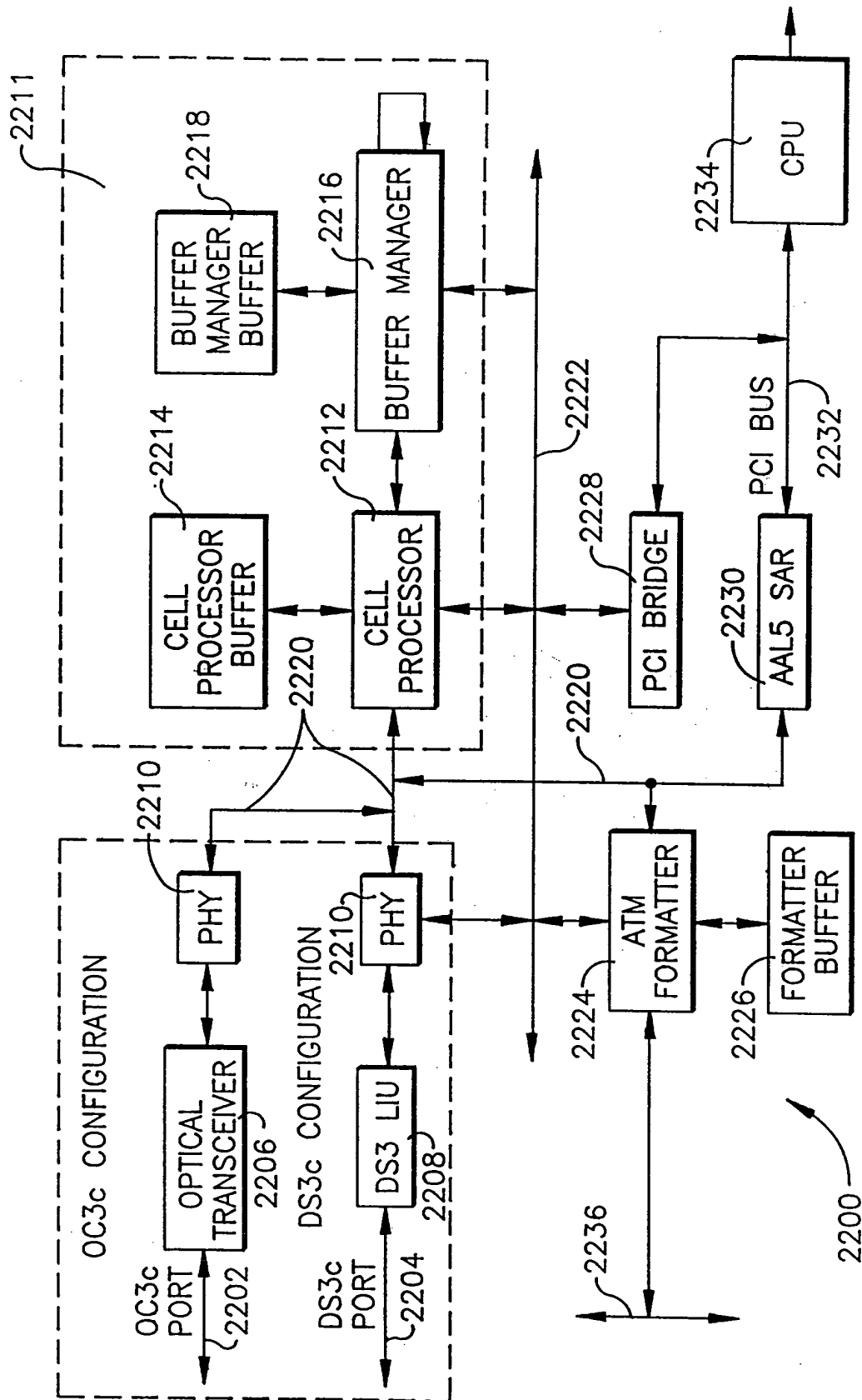


Fig. 22

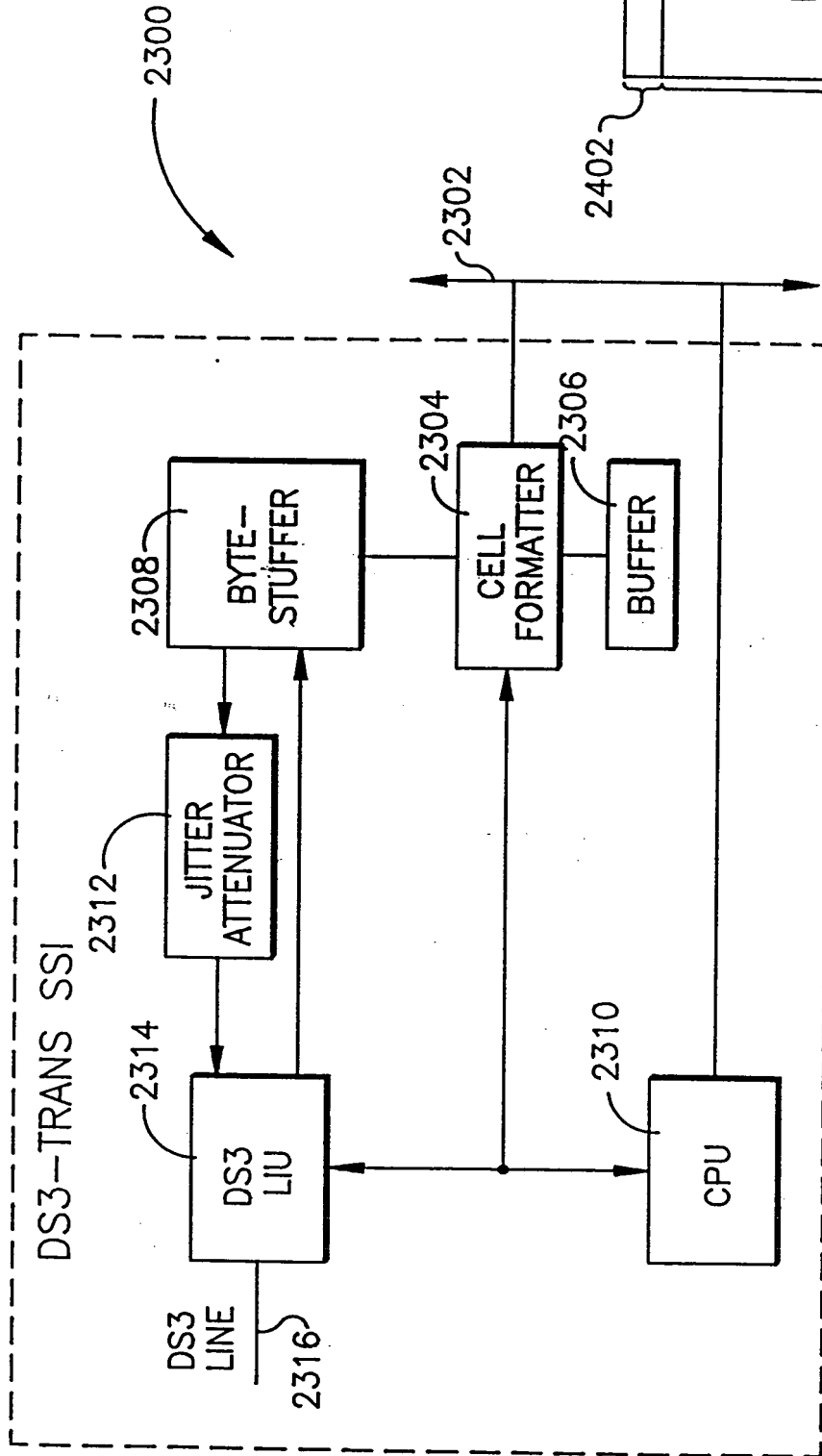


Fig. 23

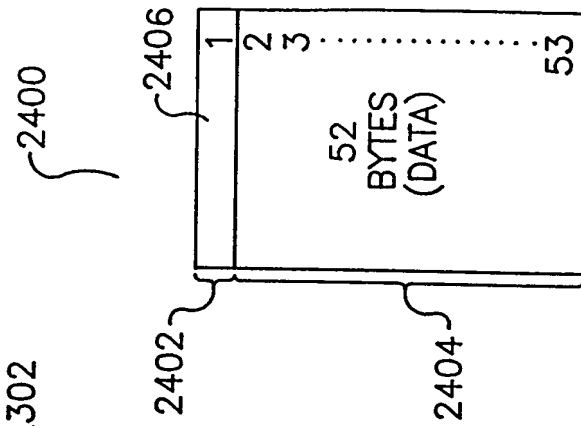


Fig. 24

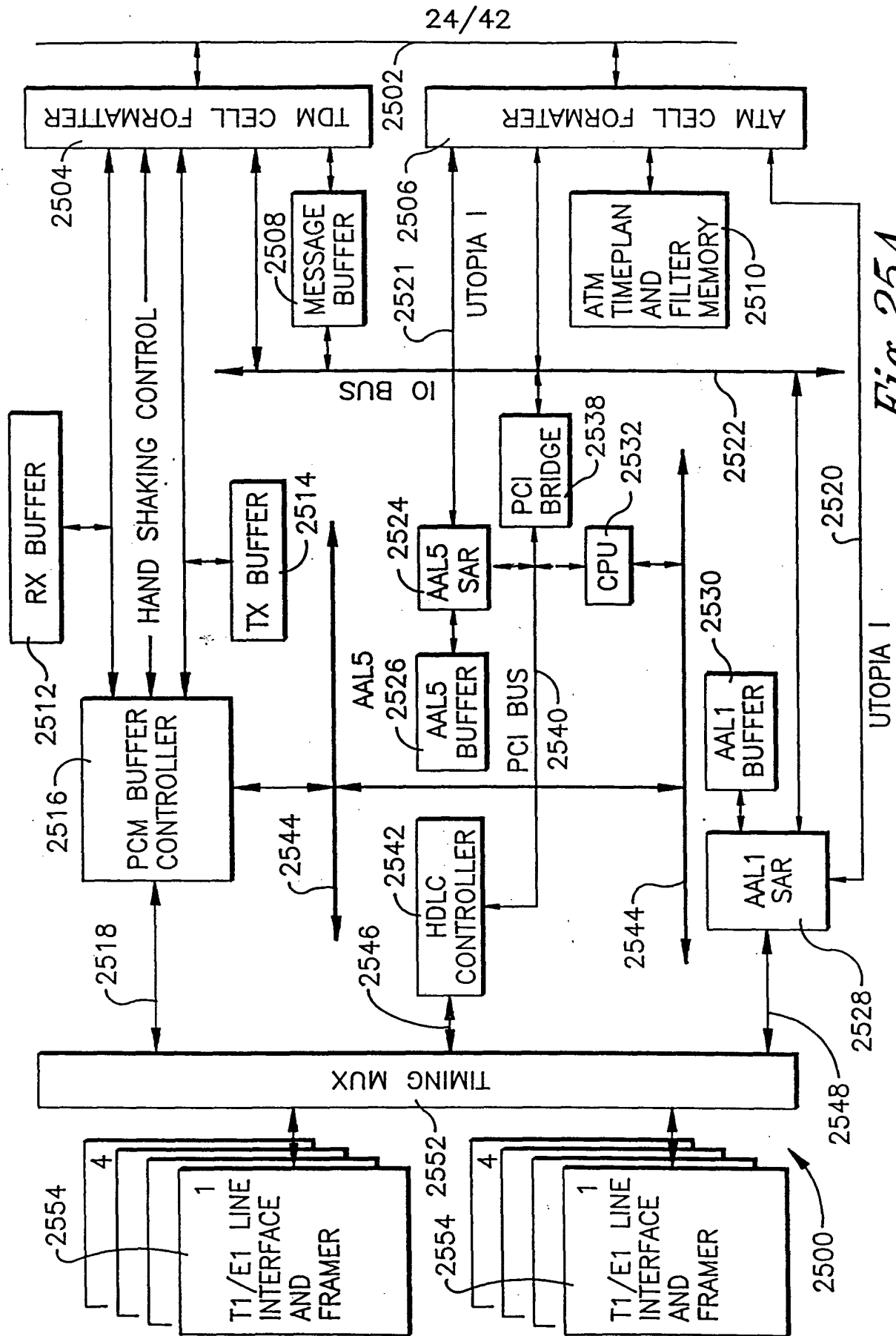


Fig. 25A

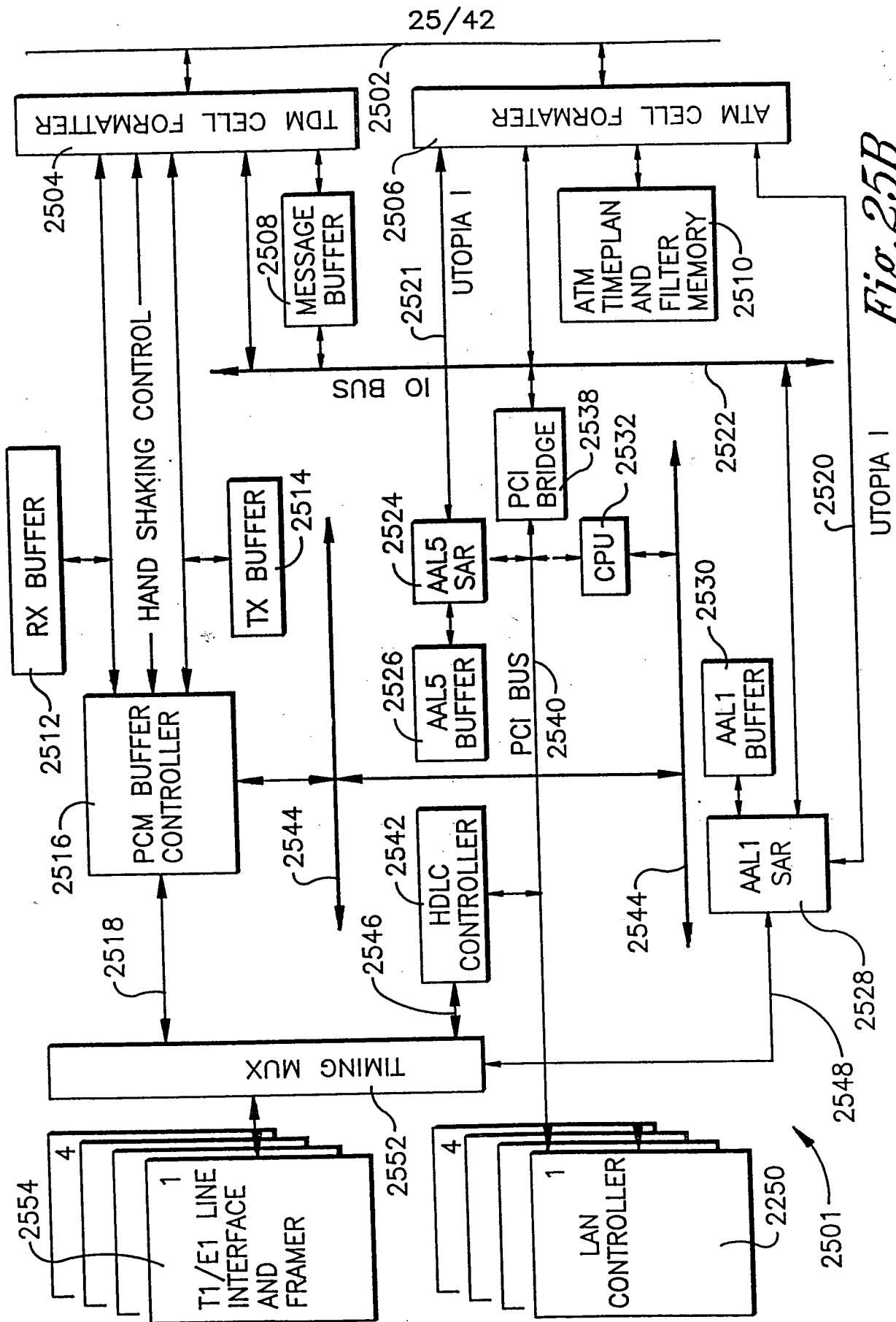
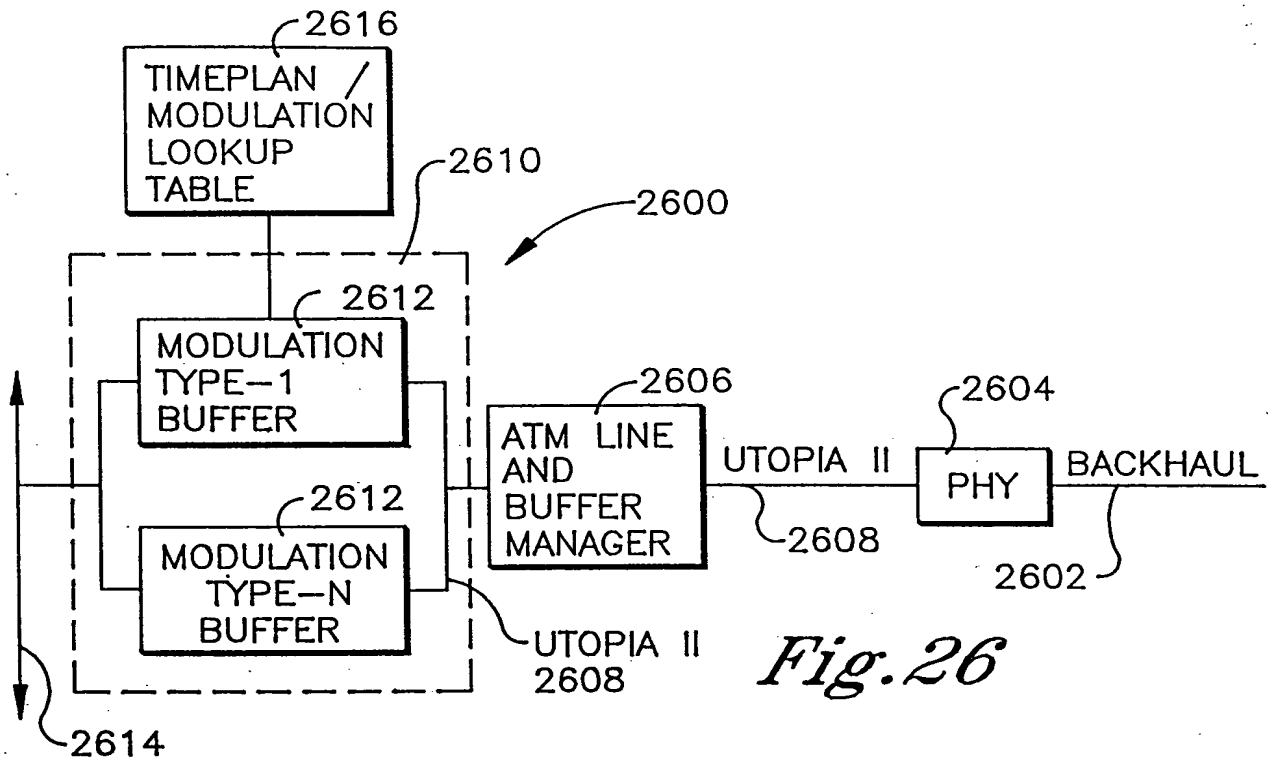
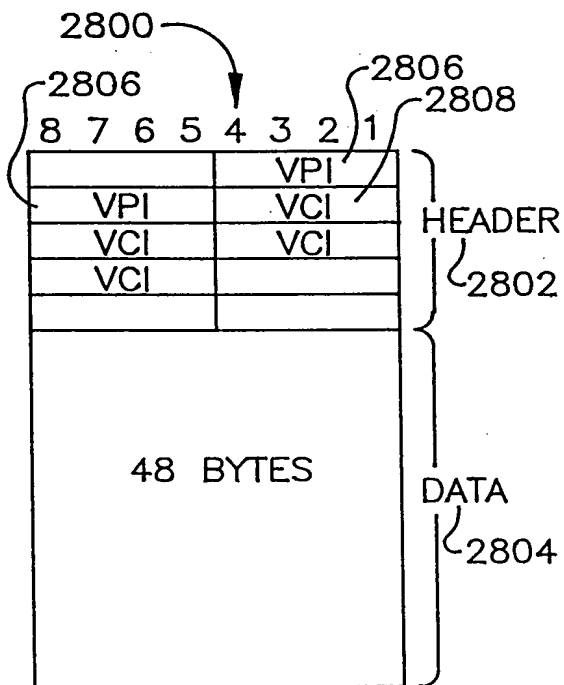
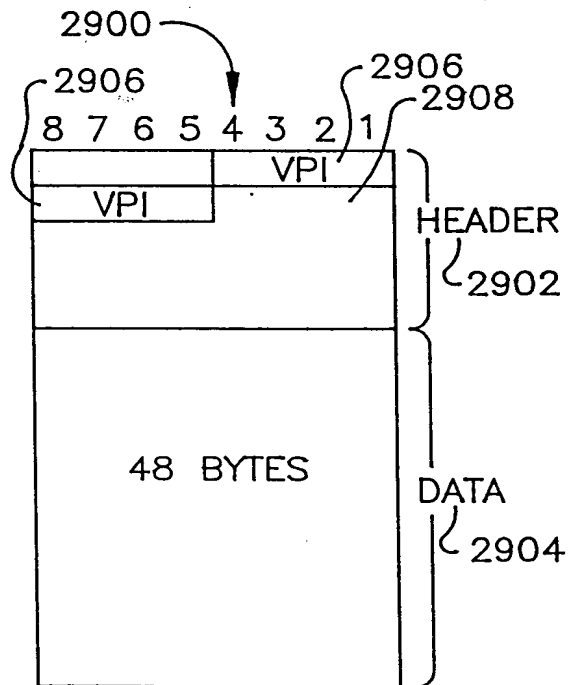


Fig. 25B

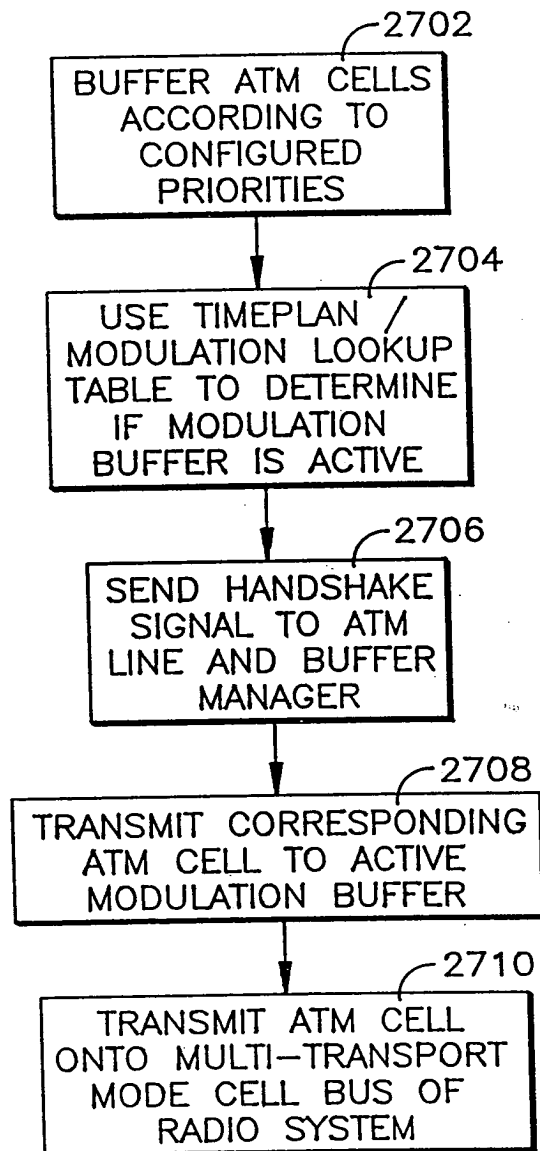
*Fig. 26*

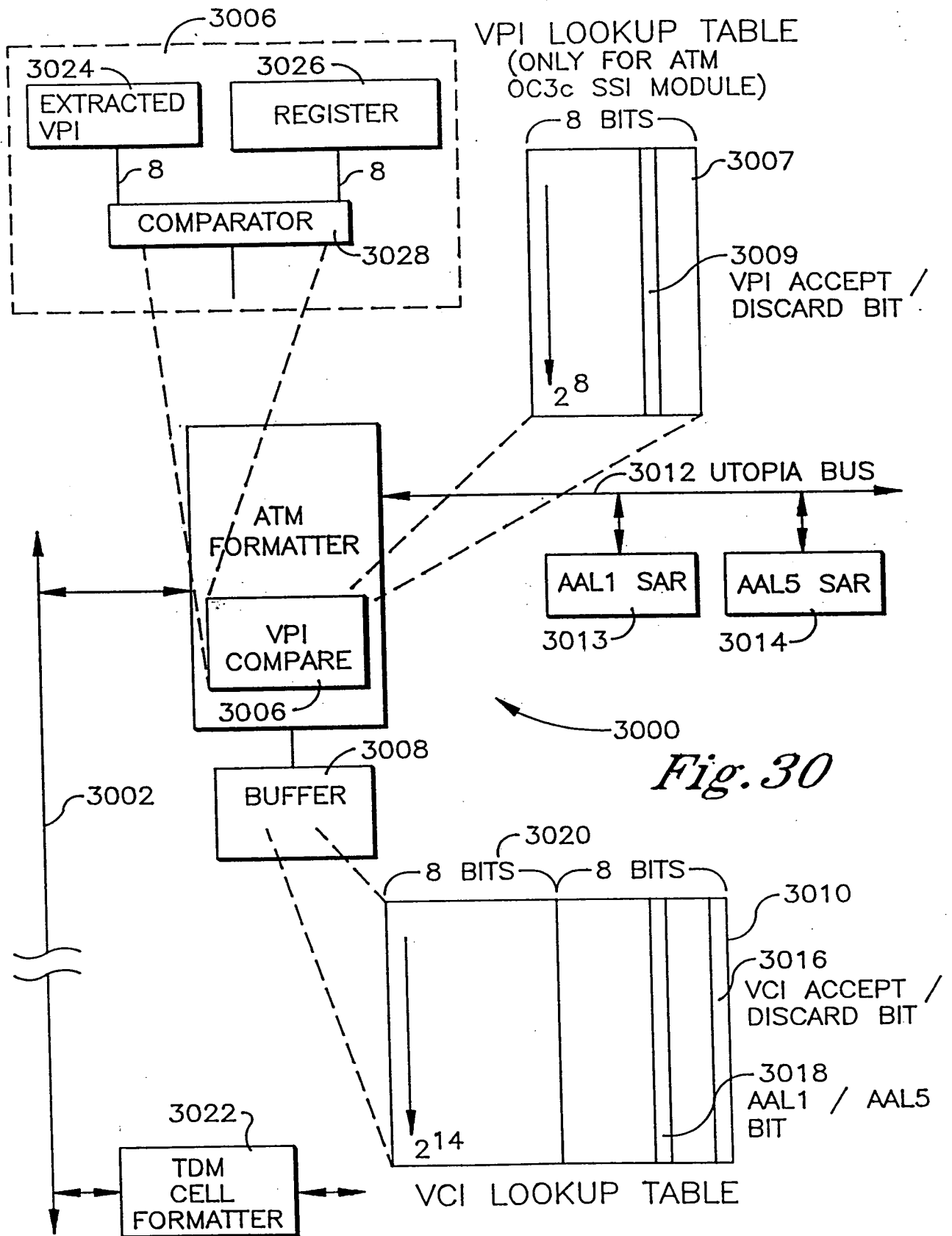
ATM CELL

Fig. 28

TDM CELL

Fig. 29

Fig. 27



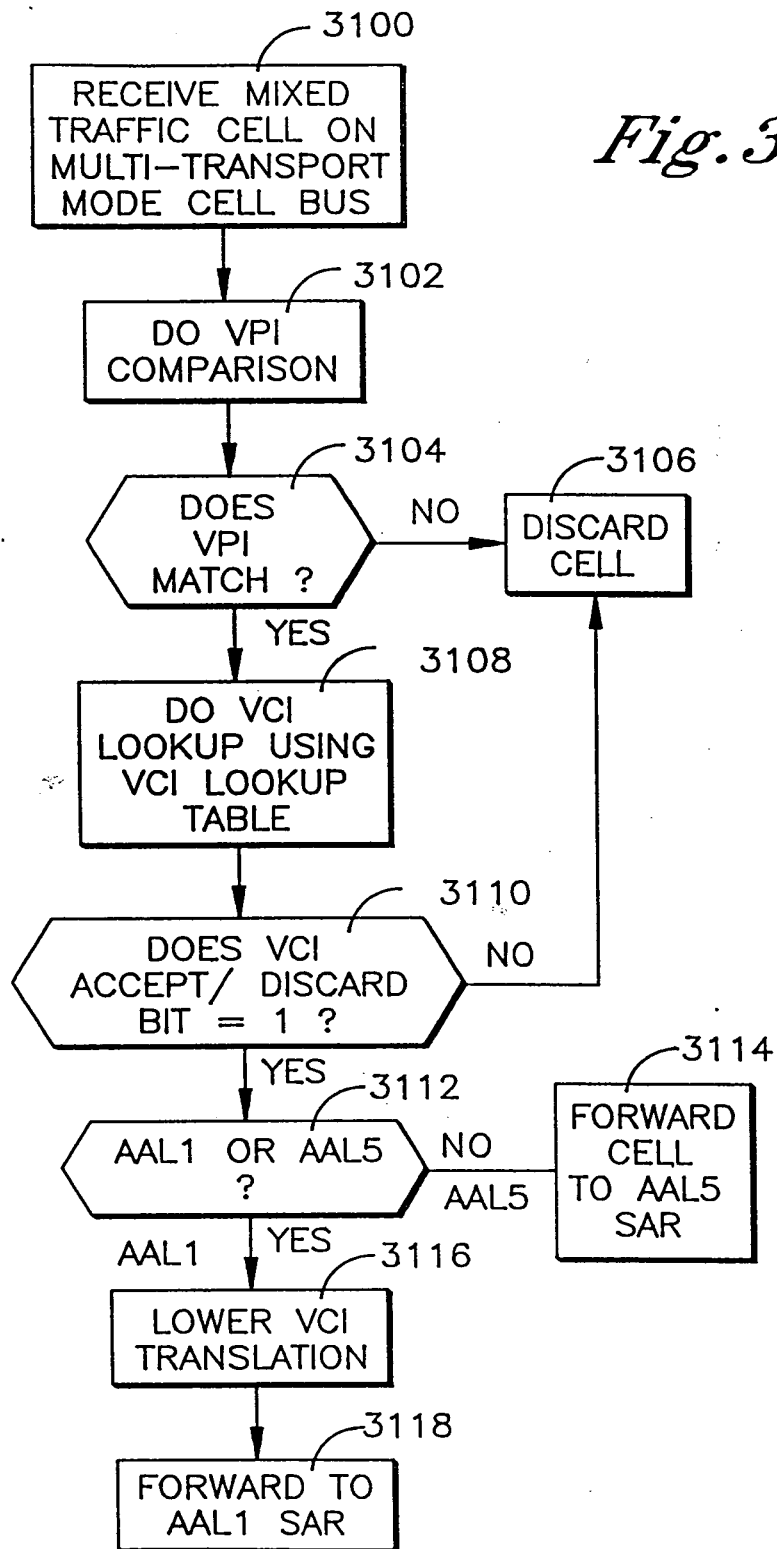
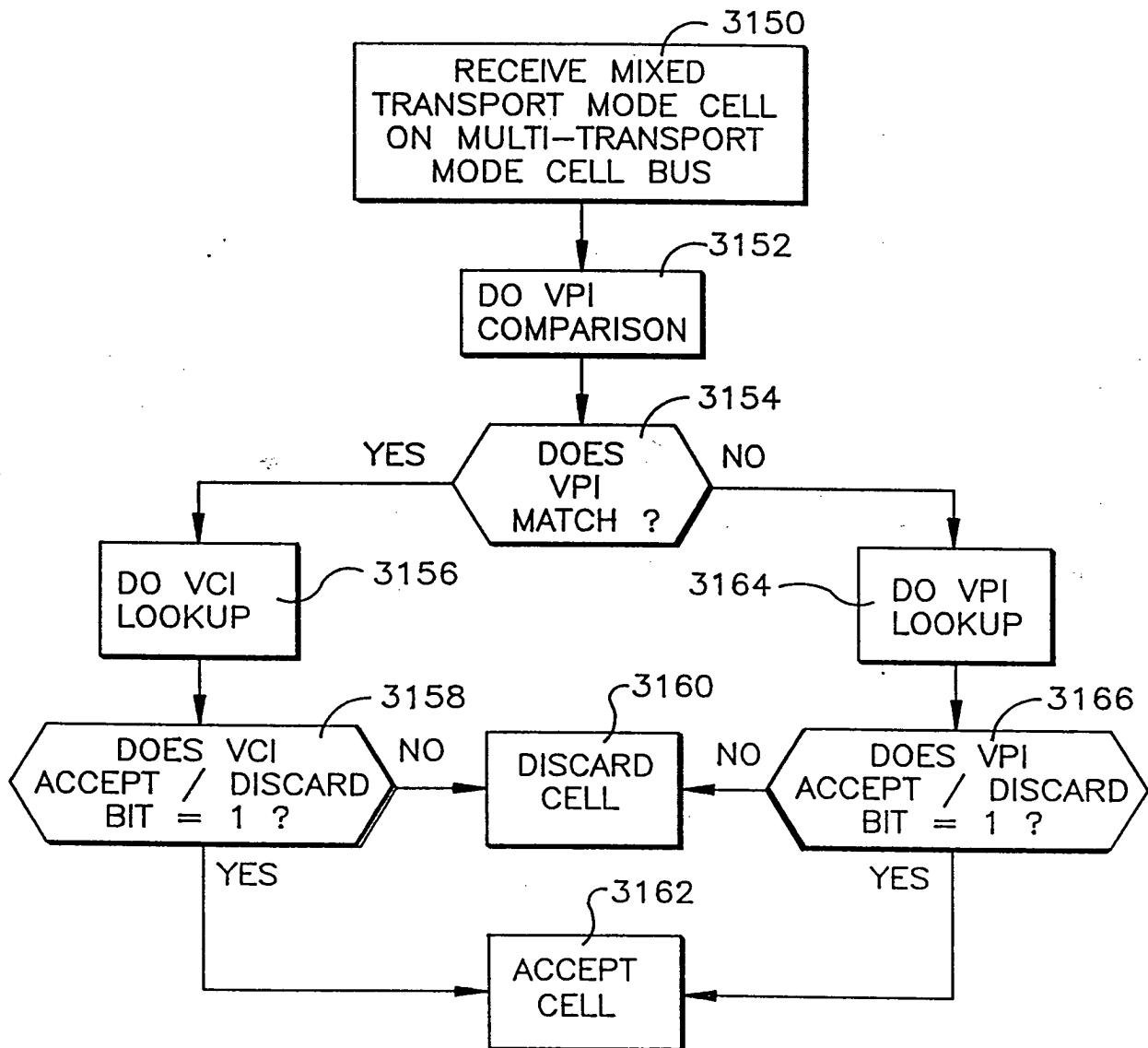
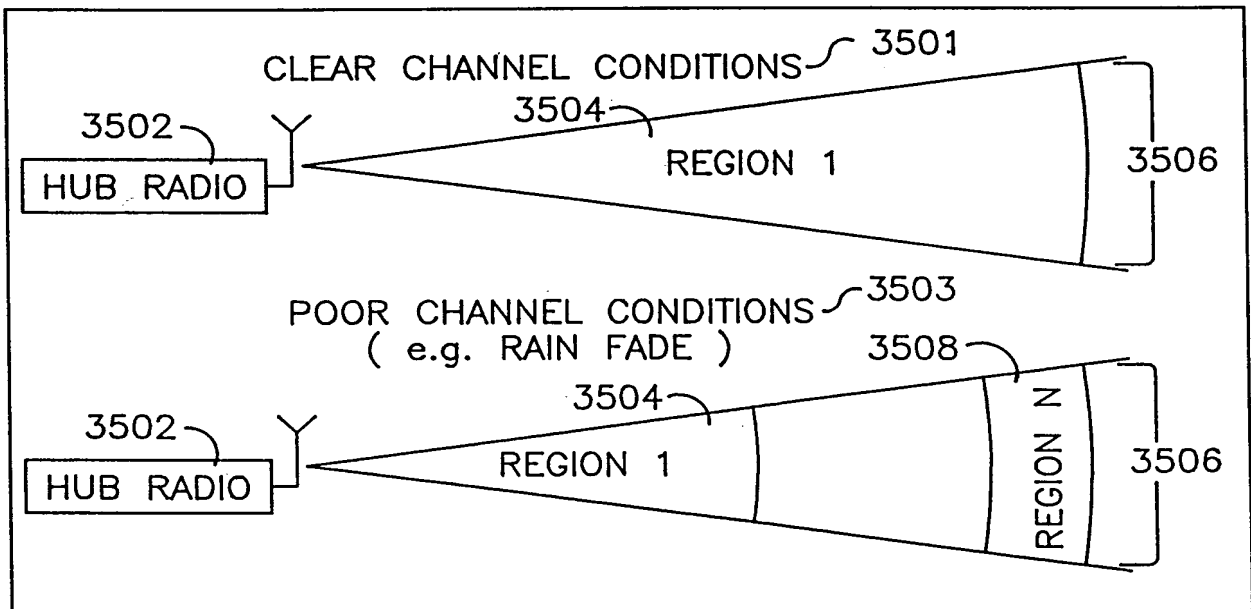
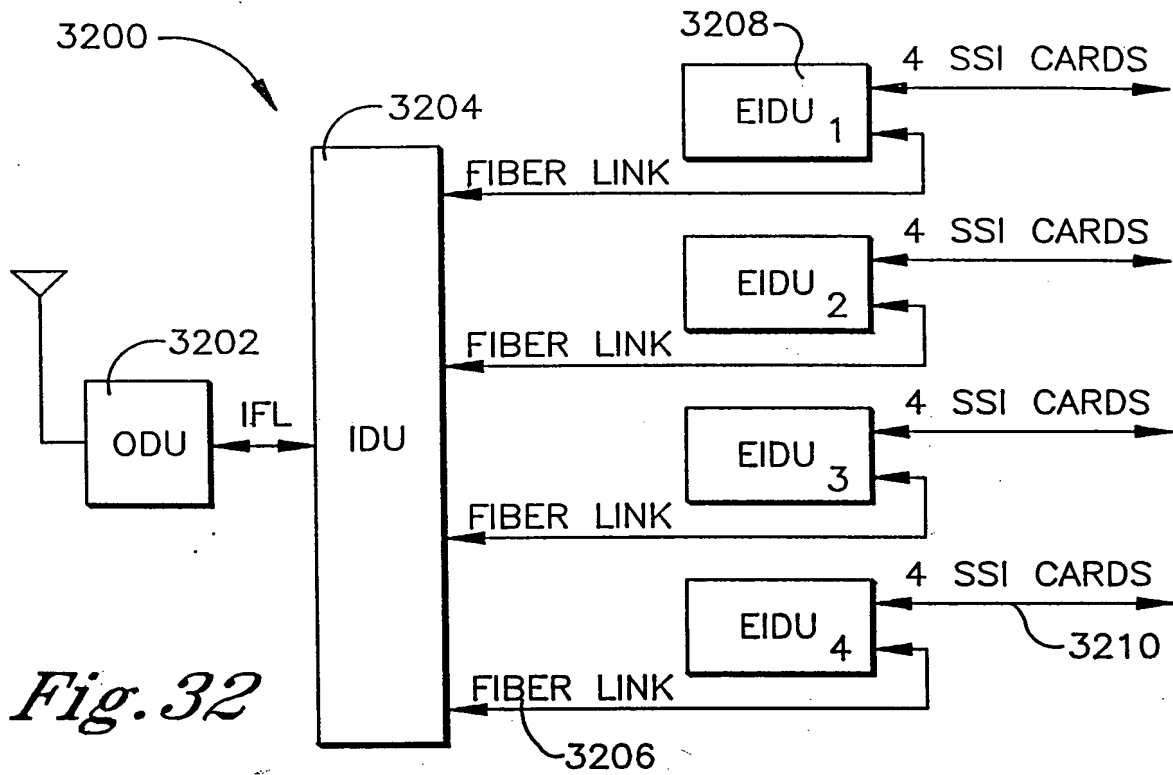
*Fig. 31A*

Fig. 31B

*Fig. 35*

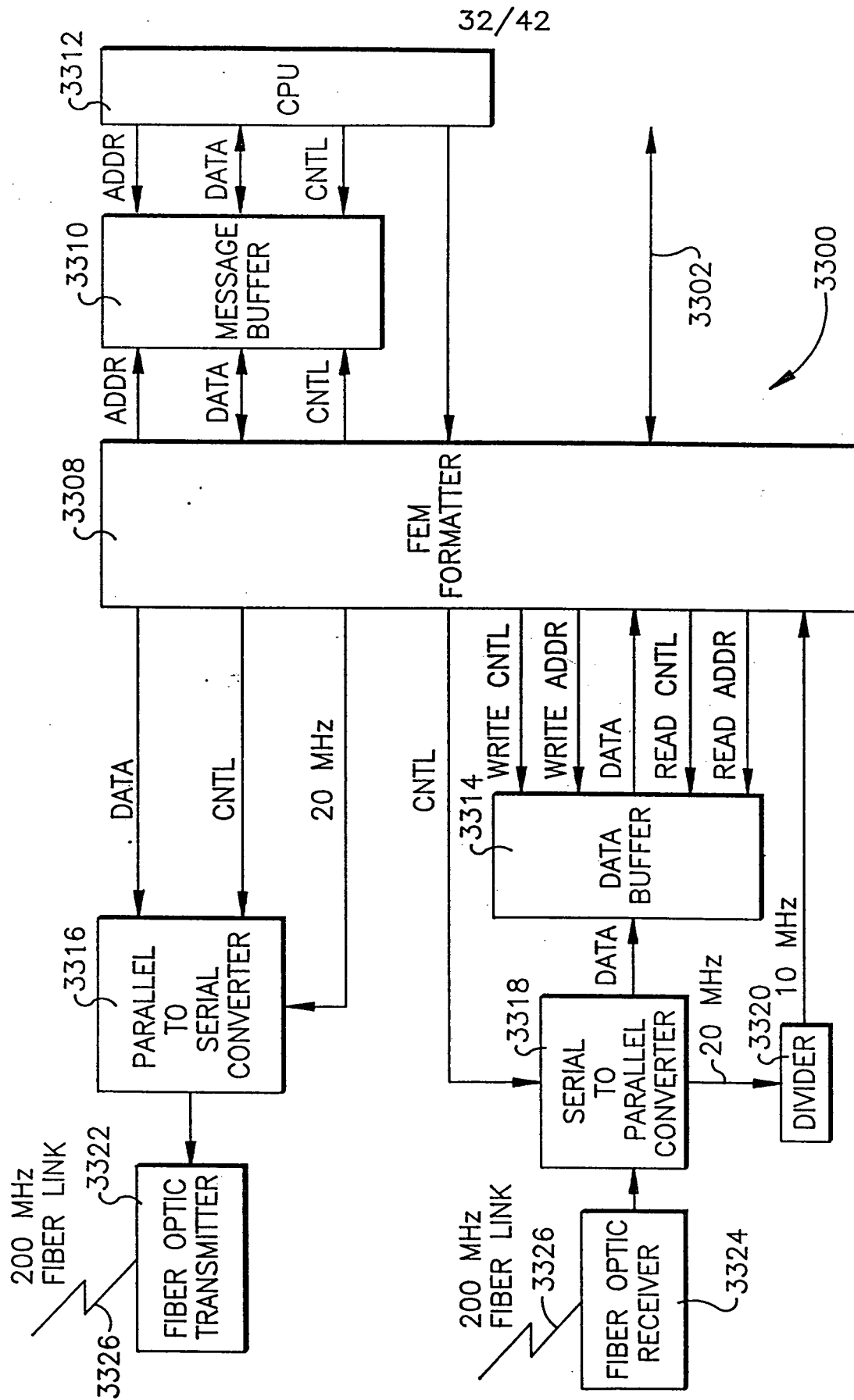


Fig. 33

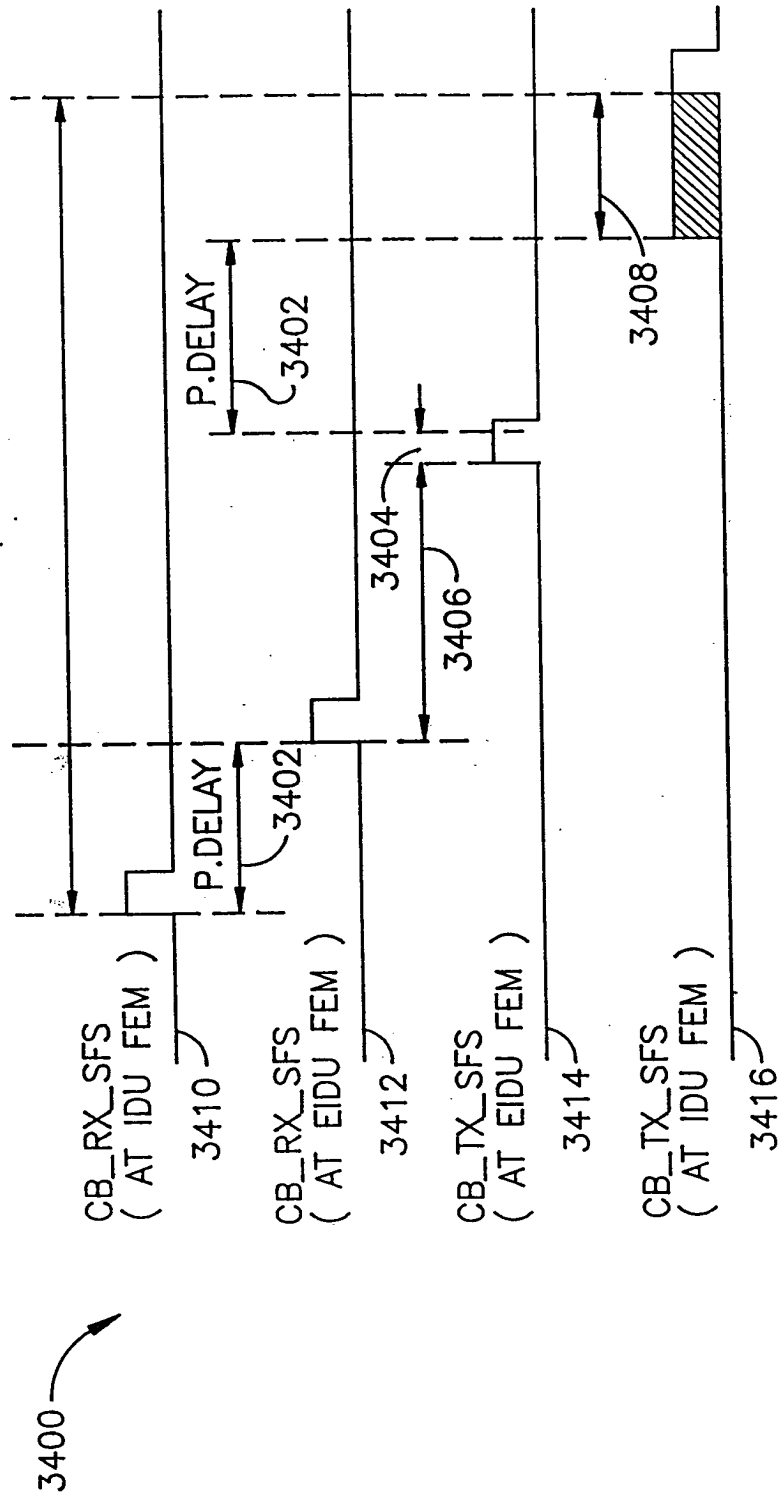
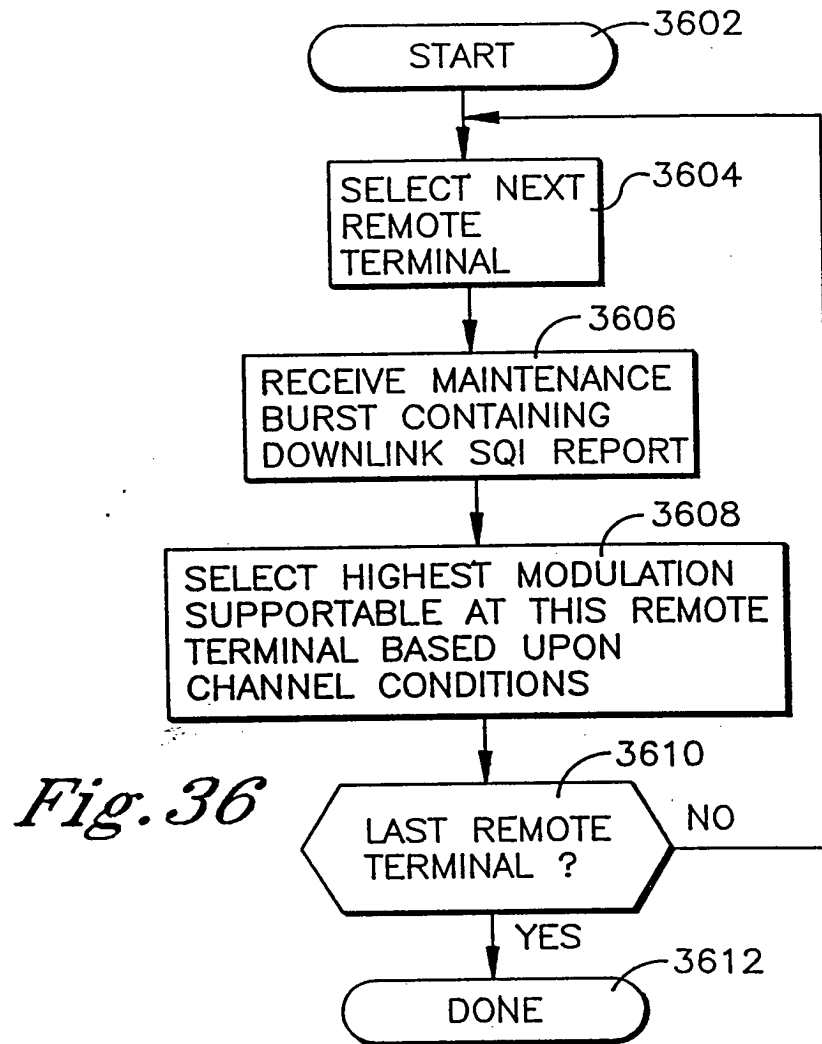


Fig. 34



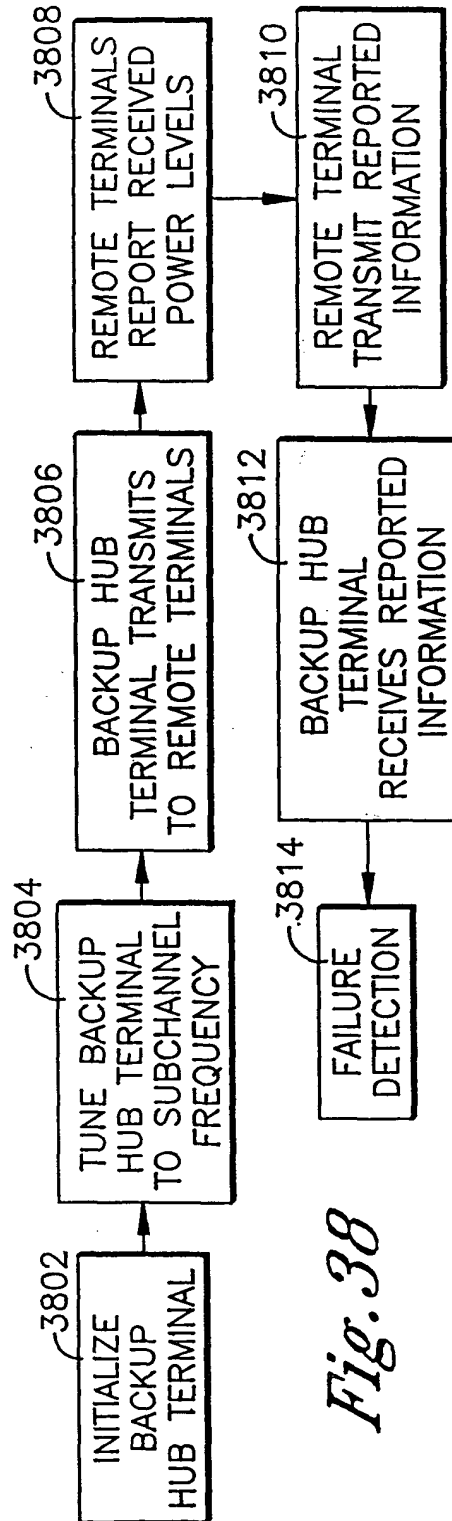
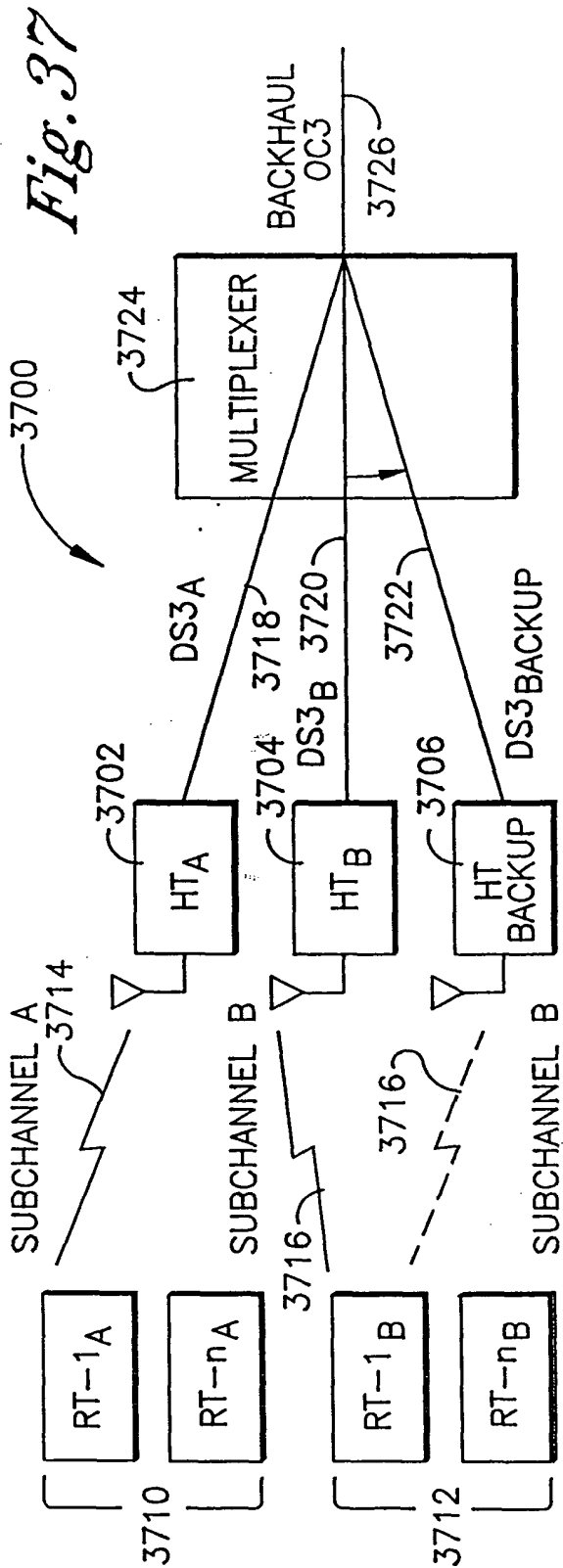
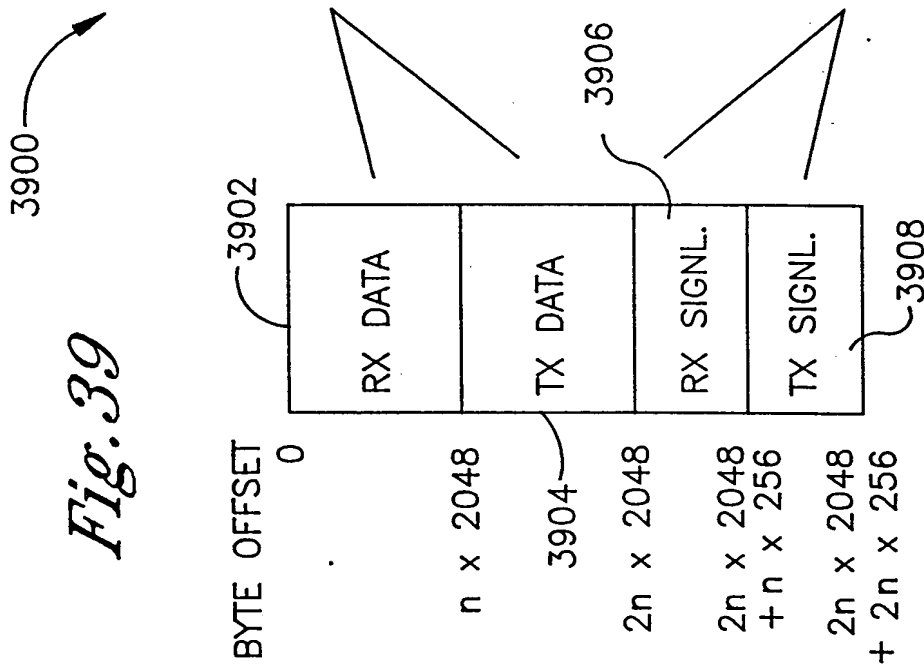
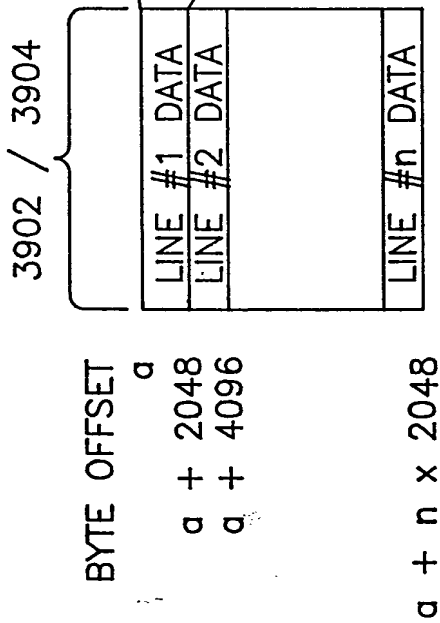


Fig. 39



n = NUMBER OF T1/E1 LINES
1 FOR SINGLE DS1 MODULE
4 FOR QUAD DS1 MODULE
32 FOR DS3 TDM MODULE



```
a = 0 FOR RX
a = a X 2048 FOR TX
```

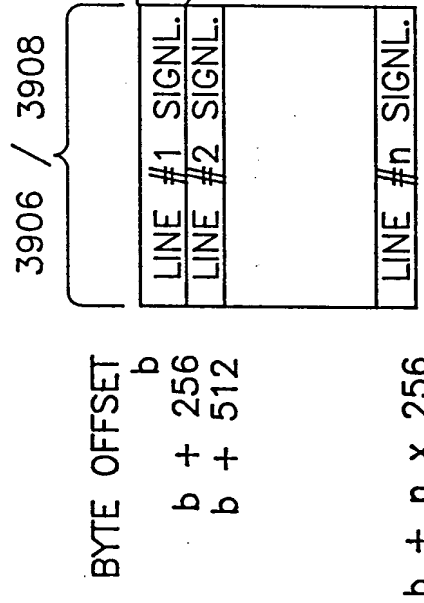
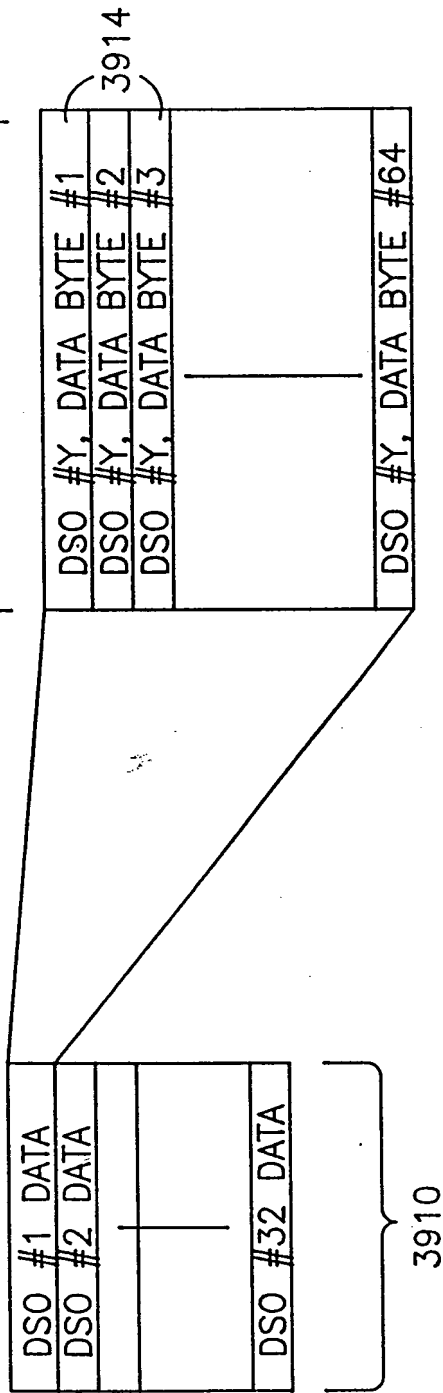

$$\begin{aligned} b &= 2n \times 2048 \text{ FOR RX} \\ b &= 2n \times 2048 + n \times 256 \text{ FOR TX} \end{aligned}$$

Fig. 39

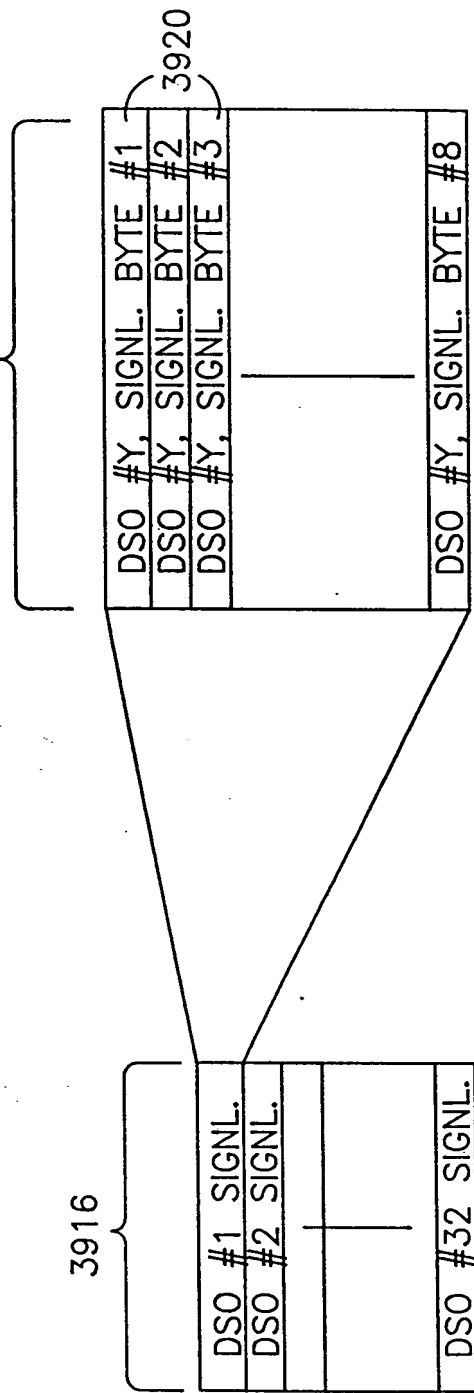
BYTE OFFSET

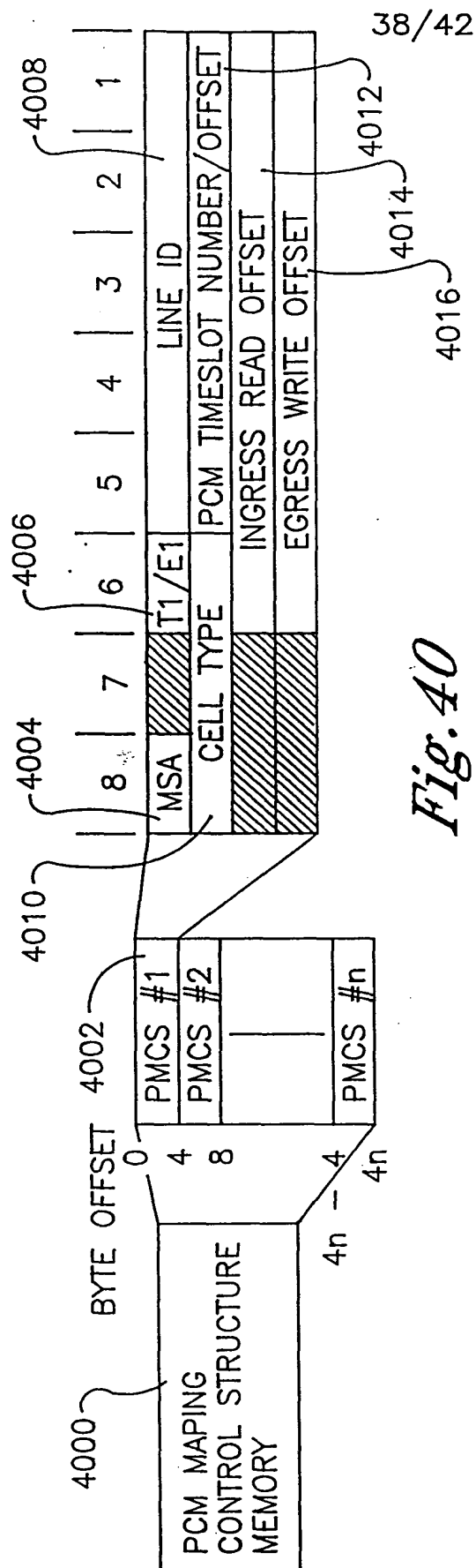
 a $a + 64$ $a + 128$ $a + 2048$ 

3918

3916

BYTE OFFSET

 b $b + 8$ $b + 16$ $b + 256$ 



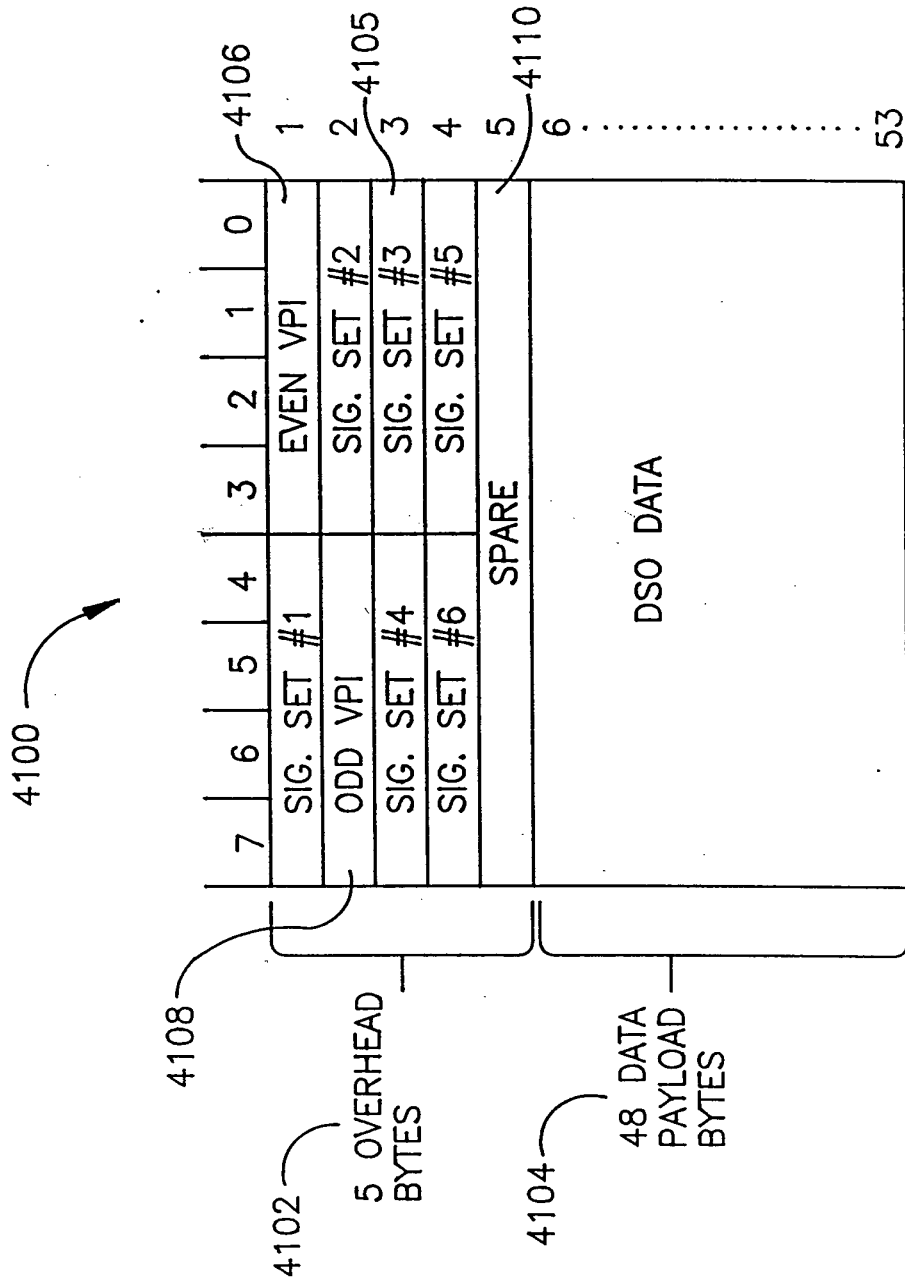


Fig. 41

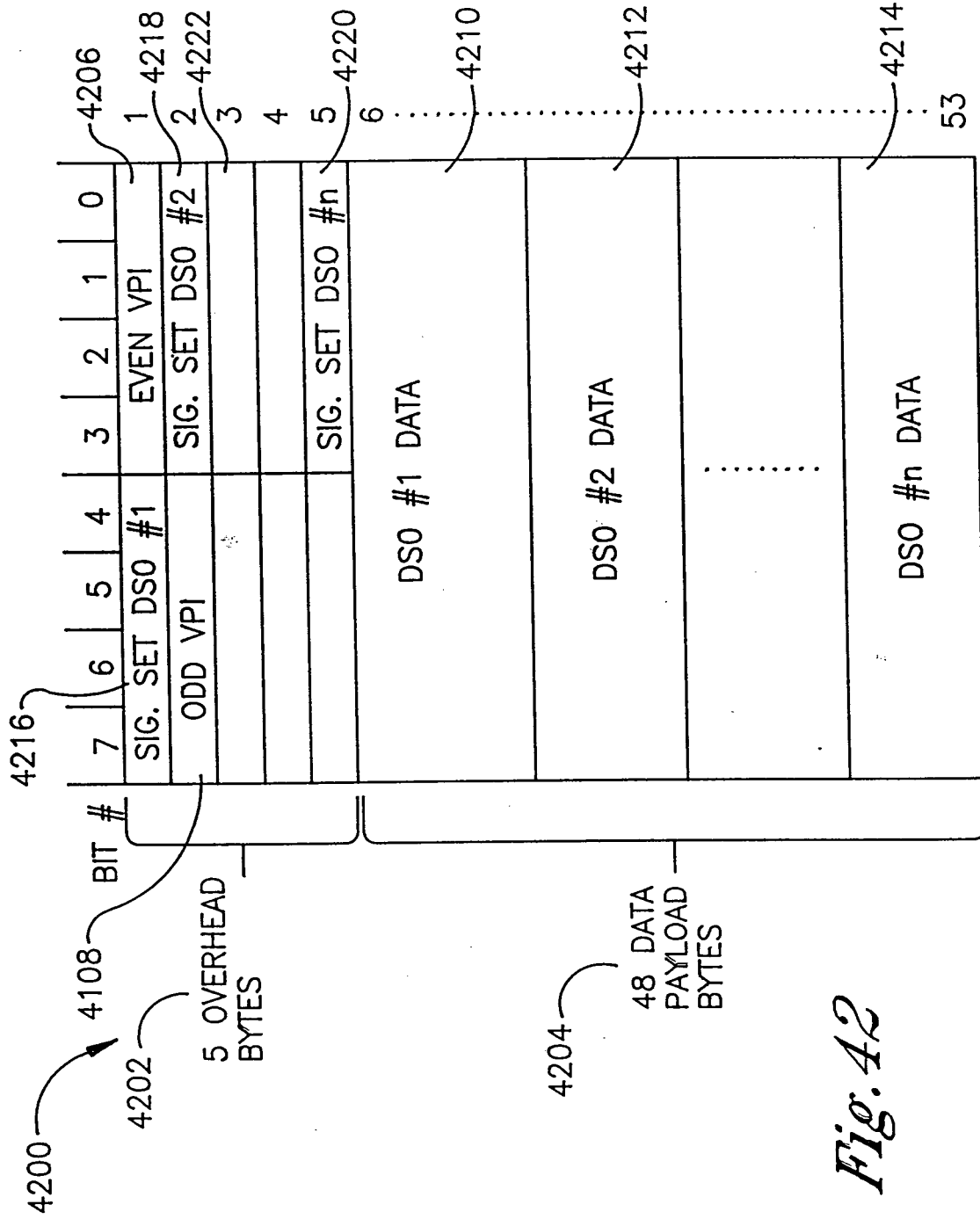


Fig. 42

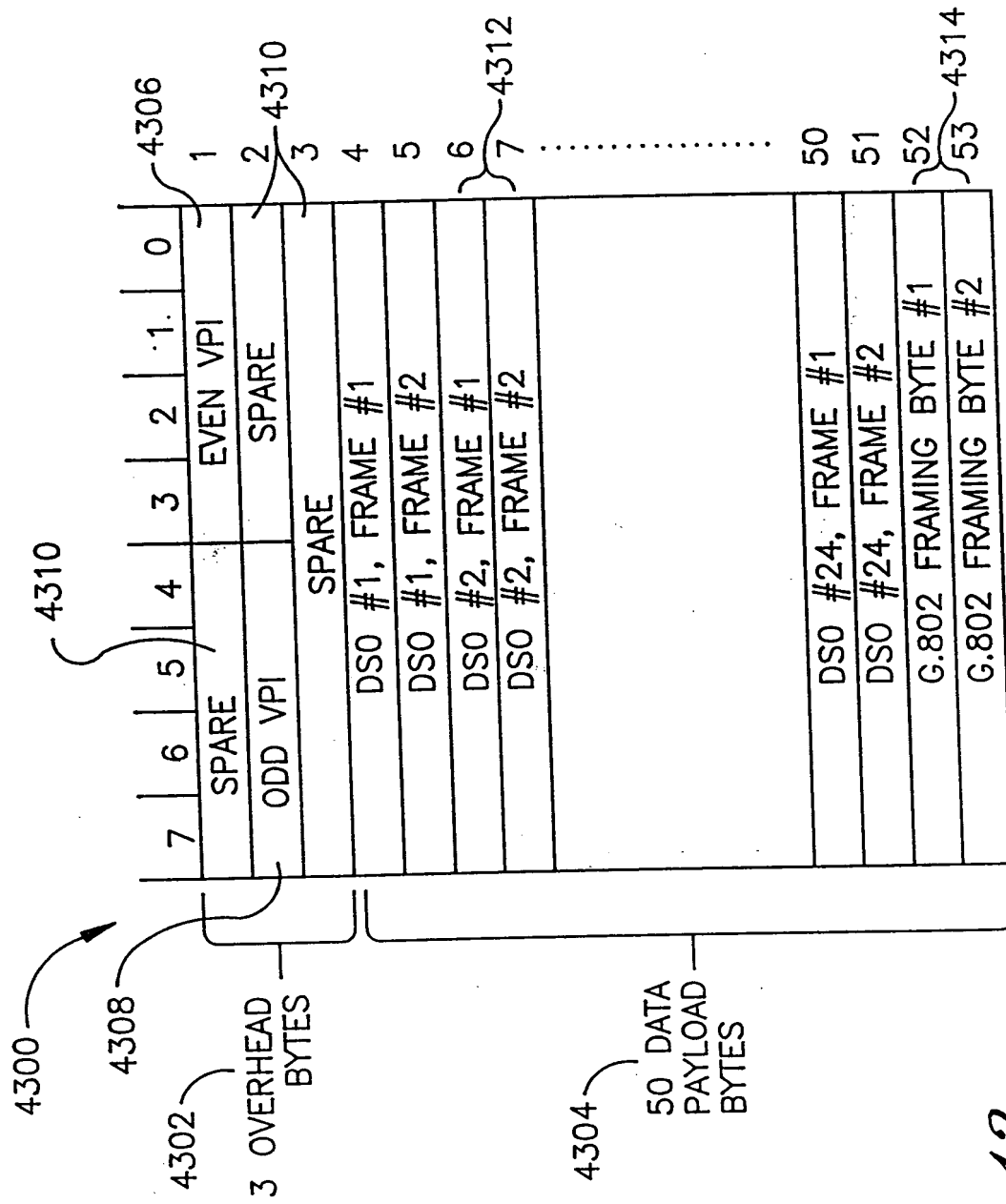
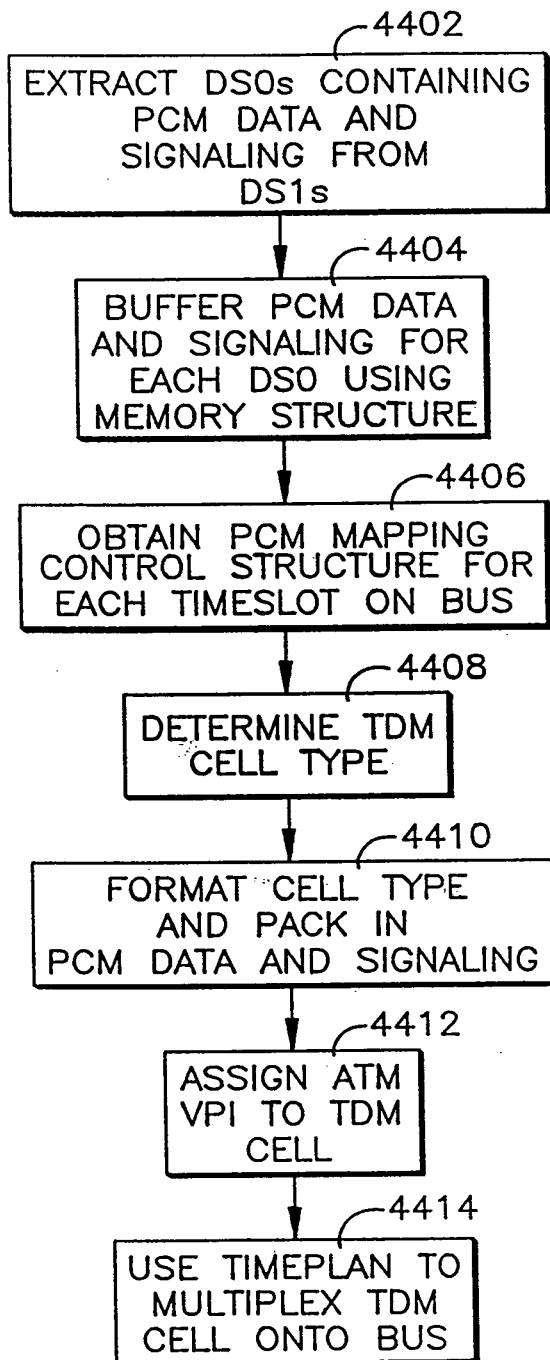
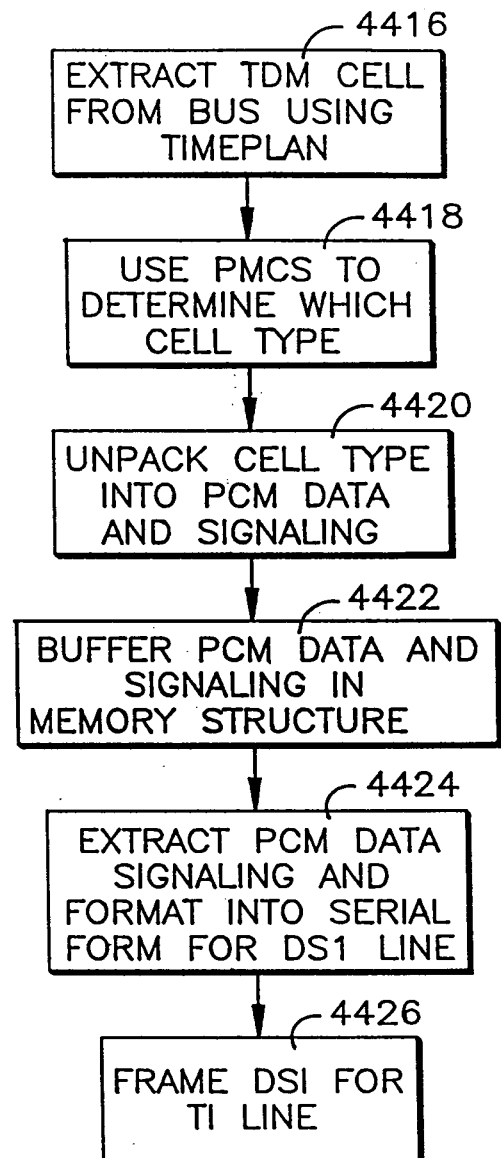


Fig. 43

*Fig. 44A**Fig. 44B*